Introduction

*Engineering : Engineering is the science of transforming knowledge in physics, chemistry and mathematics into products & system.

*Electronics : The branch of Engineering which deals with current conduction through a vacuum (or) gas (or) semiconductor is known as electronics.

*Electronic device : The device in which current flows through a vacuum (or) gas (or) semiconductor is called electronic device.

*Applications of electronics (or) Importance of electronics

① Rectification ② Amplification ③ Conversion of light into electricity ④ conversion of electricity into light etc

* Structure of Solids :

Solid (or) material (or) matter consists of atoms (or) Molecules.

* Atomic Structure :

The atoms are the building bricks of all matter. An atom consists of a central nucleus of positive charge around which small negatively charged particles called electrons revolve in different paths (or) orbits.

Nucleus consists of protons & neutrons. A proton is a positively charged particle, while the neutron has no charge.

Note: ① Matter is also known as Material.

② Four states of matter are Solid, Liquid, Gas & Plasma.

③ An atom is the smallest unit consists of proton, neutron & electron.

④ A Molecule is formed when two or more atoms join together chemically.

⑤ A Compound is a molecule that contains at least two different elements.

⑥ An atom or molecule with a net electric charge due to the loss or gain of one or more electrons, is ion

⑦ A minute portion of matter is Particle or A Particle is a small piece of anything

Ex: ① Atoms are particles for matter

② protons, neutrons & electrons are particles of an atom.

⑧ mass of the proton = mass of the neutron = 1.672×10^{-27} kg

⑨ mass of electron = 9.1×10^{-31} kg

⑩ Charge of an electron = 1.602×10^{-19} C.

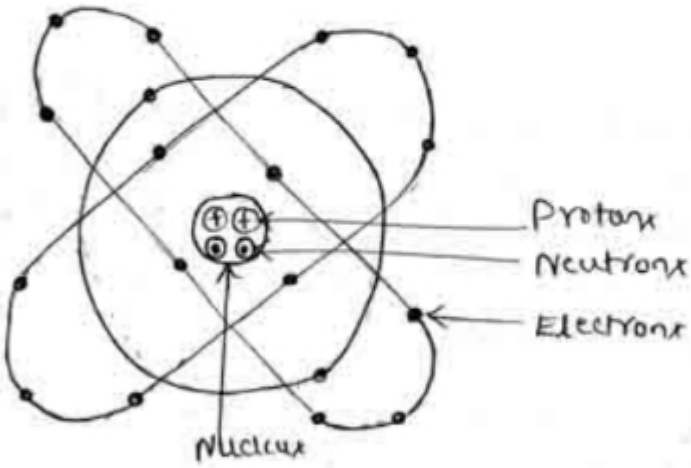
⑪ Some basic arrangement of atoms is repeated throughout the entire solid material is called crystal lattice. Such solids are called crystalline solids.

· Solid materials which donot have crystalline structure are called non-crystaline (or) amorphous solids.

Ex: All metals & elements like Silicon & germanium are crystalline materials.
Wood, Plastic, Paper, glass etc are amorphous materials

⑫ Atomic Weight (Atomic mass) = no of Protons + no of neutrons.
Atomic number = no of protons (or) electrons in an atom.

⑬ In a normal atom the number of protons = no of electrons. (Atom is neutral)

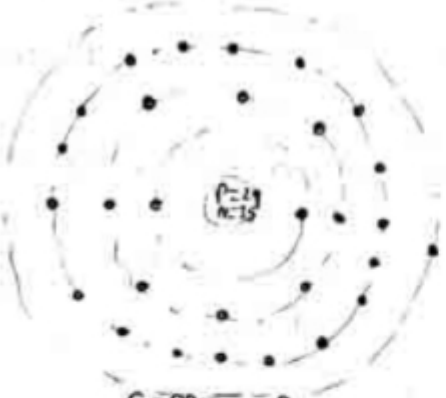


Structure of an atom.

⑭ The electrons in an atom revolve around the nucleus in different orbits (or) Paths. The number and arrangement of electrons in any orbit is determined by the following rules:

(i) The number of electrons in any orbit $= 2n^2$.
$n \rightarrow$ number of the orbit.
First orbit contains $2 \times 1^2 = 2$ electrons etc

(ii) The last orbit cannot have more than 8 electrons.
(iii) The last but one orbit cannot have more than 18 electrons.



Copper P=29
N=35
e=29

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*Energy of an electron:

An electron moving around the nucleus possesses two types of energies viz. kinetic energy due to its motion & potential energy due to the charge on the nucleus. The total energy of the electron is the sum of these two energies.

The energy of an electron increases as its distance from the nucleus increases. The electron in the last orbit possess very high energy as compared to the electrons in the inner orbits.

* Electron orbits:

The orbits are represented by the letters K, L, M, N etc counted from the nucleus to outwards. Sometimes K, L, M, N etc are also designated as 1, 2, 3, 4 etc

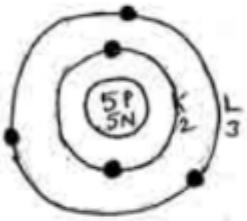
* Distribution of electrons in atoms

→Atomic number of boron is 5.

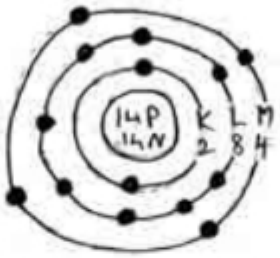
It has 5 protons & 5 electrons.

Two electrons occupy the K-shell, which is then said to be completely filled. The other 3 electrons occupy the L-shell as shown in fig①

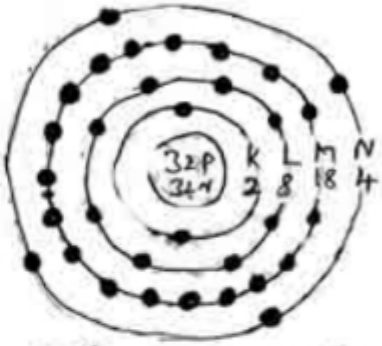
→Atomic number of Silicon is 14.



Fig①: Boron(B)



Fig② Silicon(Si)



Fig③: Germanium(Ge)

It has 14 protons and 14 electrons.

2 electrons occupy the K-shell, 8 in L-shell & 4 in the M-shell as shown in fig②.

→ Atomic number of germanium is 32.

It has 32 protons and 32 electrons.

2 electrons occupy the K-shell, 8 in L-shell, 18 in M-shell and 4 in N-shell as shown in fig③

Note:

① Each electron orbit (main shell) in an atom consists of no of sub-orbits ② Sub-shells. The no of sub-orbits is equal to the no of its Principal Quantum no(n).

Ex: K-shell → one sub-orbit
L shell (n=2) → 2 sub-orbits
M shell (n=3) → 3 sub-orbits etc

* Energy possessed by an electron in the orbit

→ Some energy is emitted by an electron, when it moves from a higher orbit to a lower orbit.

→ Similarly, some energy is absorbed by an electron when it moves from a lower orbit to a higher orbit.

→ The amount of energy emitted (or absorbed) is,

$$W_2 - W_1 = hf \text{ Joules}$$

- Where, W_2 → Energy of the initial orbit
- W_2 → Energy of the final orbit.
- h → Planck's constant = 6.626×10^{-34} Js
- f → frequency of radiation.

→ The total energy (both Kinetic and Potential) possessed by an electron, when it revolves in the nth orbit of an atom, with atomic number Z, is.

$$W_n = -21.76 \times 10^{-19} \frac{Z^2}{n^2} \text{ Joules}$$

→ Energy of an electron (in electron volts) is.

$$E_n = \frac{-21.76 \times 10^{-19}}{1.6 \times 10^{-19}} \frac{Z^2}{n^2} = -13.6 \times \frac{Z^2}{n^2} \text{ eV}$$

Smaller unit of energy is electron Volt.

$$1 \text{ eV} = 1.602 \times 10^{-19} \text{ Joule}$$

* Energy levels & Energy level diagram:

→ Electrons can occupy only certain orbital shells at fixed distances from the nucleus.

→ The electrons in the outer shell determine the

electrical and chemical properties of a material.

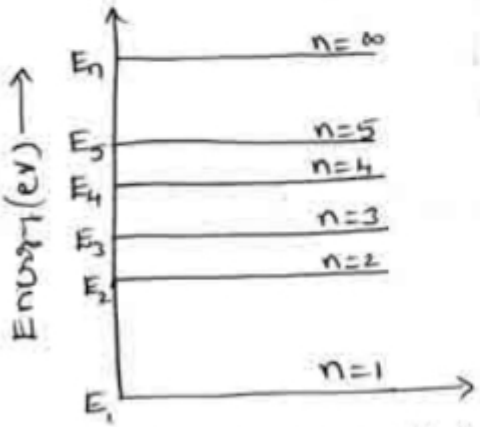
→ The closer an electron is to the nucleus, the stronger are the forces that bind it to the atom.

→ Each shell has an energy level associated with it that represents the amount of energy required to extract an electron from the atom.

→ Least amount of energy is required to extract the electrons from valence shell.

→ Greatest energy is required to extract the electron from the orbits which are closest to the nucleus.

→ The diagram in which we plot the energies corresponding to K, L, M... etc shells is known as energy level diagram (fig *)



Fig(*) : Energy level diagram

→ When the electron is present in the first orbit (n=1), it is said to be in its normal ground state.

→ If the electron is present in the higher orbits, it is said to be in the excited state.

Note:

① Interatomic bonds: The bond formed between the atoms in the solid (interatomic forces) is called Interatomic bond.

② Ionic bond: The bond formed between two oppositely charged ions, which are produced by the transfer of electrons from one atom to another, it called ionic bond

(B) Electrovalent bond.

⑤ Covalent Bond: The bond which is formed by the sharing of electrons between two atoms, it called Covalent bond.

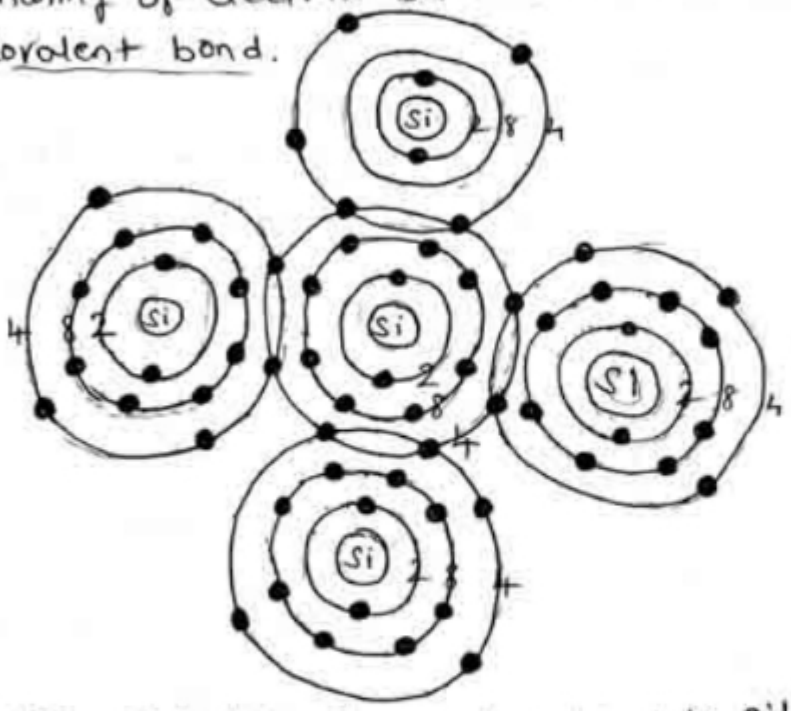


Fig: Formation of Covalent bond in Silicon Crystal

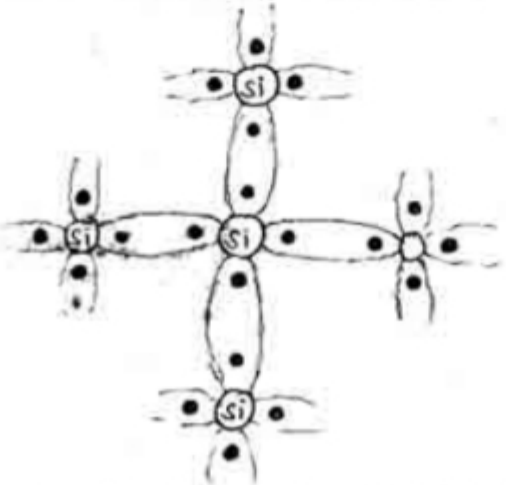


Fig: Covalent bond in Silicon Structure

④ Metallic bond:

In metal atoms, the electrons in the outermost shells are loosely held by their nuclei. So electrons in the outermost shell require a very small amount of energy to detach themselves from their nuclei. At room temp, all the metal atoms lose their outermost shell electrons, which form an electron cloud @ common pool of electron. These electrons have a freedom to move only where within the crystal. The atoms, after losing their outermost shell electrons, acquire positive charges and become positive ions. The electrostatic force of attraction b/w the electron cloud and positive ions forms a bond. Known as Metallic bond. (It takes place in metals only)

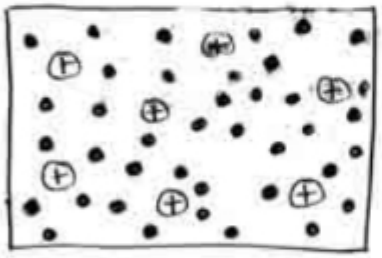


Fig: Metallic bond

⑤ Energy bands:

→ The energy levels form continuous bands of allowed energy, which the electrons may occupy.

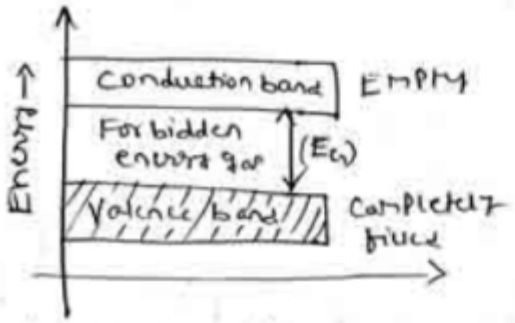


Fig: Energy level diagram

→ Each band consists of a large number of very closely spaced discrete energy levels. (The range of energies possessed by an electron in a solid is known as energy band)

* **Valence electrons :**

The electrons in the outermost orbit of an atom are known as Valence electrons

* **Free electrons:**

The valence electrons which are very loosely attached to the nucleus are known as free electrons.

The free electron can be easily removed (or) detached by applying a small amount of external energy

* **Classification of Solids (Materials):**

Based on electrical properties, materials are generally classified into Conductors, insulators and Semiconductors.

① **Conductor:** (Metal)

→ No of valence electrons of an atom is less than 4. Ex: Sodium, magnesium, aluminium etc

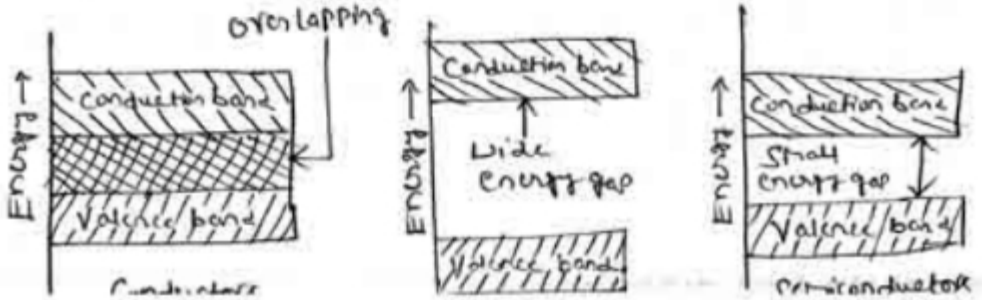
→ Large no of free electrons exists.

→ When P.d is applied across a conductor, the free electrons move towards the positive polarity of supply constituting electric current.

→ Positive temperature coefficient of resistance

→ Conduction & valence bands overlap.

→ Resistance is in the order of $10^{-6}\Omega$.



② Insulators: (Non-metal) (Dielectric materials)

→ No of Valence electrons of an atom is more than 4.

Ex: Nitrogen, Sulphur, neon etc

→ Insulator has practically no free electrons at ordinary temperature.

→ Conduction and Valence bands are separated by a wide energy gap (≈15 eV)

→ have very high resistivity ($10^{14}\Omega$) & low conductivity.

→ If temperature is raised, some of the Valence electrons may acquire energy and jump into the conduction band. & hence resistivity decreases. (negative temperature coefficient)

③ Semiconductors:

→ No of Valence electrons of an atom is 4.

Ex: Carbon, Silicon, germanium etc

→ Very few electrons at room temperature

→ Very small energy gap (≈ 1eV)

→ Resistivity is of the order 10^{-4} to 0.5 Ω m. (lab)

→ Conductivity & resistivity lies b/w insulators & conductors.

→ Small amount of energy is required to free the electrons by moving them from the Valence band into the Conduction band.

→ behave like insulators at 0K (no electrons in the Conduction band). However at room temp, a significant

No of electrons are available in the conduction band.

→ Semiconductors also have negative temperature coefficient of resistance.

Note:

① Voltage source

There are two types of voltage sources, namely

(i) Direct voltage source (ii) Alternating voltage source

Ex: Cell, dc generator

Symbol: 

Ex: AC generator

Symbol: 

② current source

③ Electric current: The movement of electric charge is called an electric current, denoted by I (A)

The conventional current flow is opposite to electron flow.

④ Passive elements

(i) Resistance (Ω)

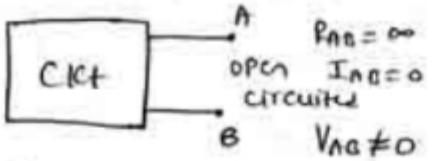
(ii) Capacitance (F)

(iii) Inductance H

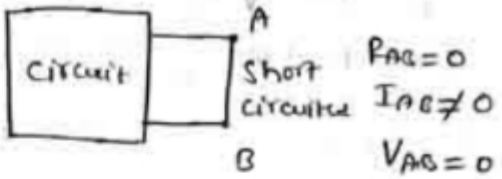
⑤ Conductance. $G = \frac{1}{R}$ · Siemens (S) or mho

Conductivity · $\sigma = \frac{1}{\rho}$ (S/m) or (℧/m)

⑥ Open and Short circuits



Open circuit



Short circuit

⑦ Kirchhoff's laws:

① Kirchhoff's current law (KCL):

"In any network, the algebraic sum of currents at any junction is zero"

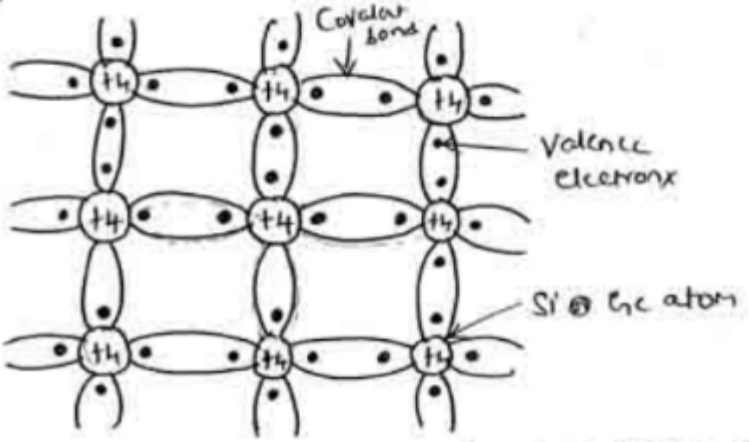
② Kirchhoff's Voltage law:

"In any network, the sum of all the voltages around a closed path (or a loop) is zero".

Types of Semiconductors

① Intrinsic ② Extrinsic

① Intrinsic: A Semiconductor which is in its extremely pure form is known as an intrinsic or pure semiconductor.



Two dimensional representation of a Silicon or a germanium

→ At 0K @ 273°C (Absolute zero temperature)

All the Valence electrons are tightly held by the Parent atoms., therefore they cannot conduct electricity.

→ At 27°C @ 300K (Room temperature)

Some of the covalent bonds are broken, the electrons are free to move anywhere within the crystal. & hence vacancies (holes) are created. therefore they conduct current.

② Extrinsic : The Semiconductors which are obtained by adding a certain amount of desired impurity atoms to pure semiconductor are called Extrinsic Semiconductors

Depending upon the type of impurity added, extrinsic Semiconductors are classified into.

(i) n-type (ii) p-type

(i) n-type: The Semiconductors which are obtained by adding pentavalent atoms (ie atoms containing 5 valence electrons) are known as n-type semiconductors

Ex: of pentavalent impurities are arsenic (As), antimony (Sb), Phosphorus (P), & Bismuth (Bi) [Donor]

(ii) p-type : The Semiconductors, which are obtained by adding trivalent impurity atoms (ie atoms containing 3 valence electrons) are known as p-type semiconductors

Ex: of trivalent impurities are gallium (Ga), indium (In), aluminium (Al), Boron (B) etc [Acceptor]

Note:

① In an n-type material, the electron is called the majority carrier and the hole the minority carrier.

② In a p-type material, the hole is the majority carrier and the electron is the minority carrier.

③ The current produced due to drifting of free electrons is called drift current (when voltage is applied)

④ The current produced due to diffusion (charge carrier move from high charge density to the low carrier(charge) density) is called diffusion current (without voltage)

⑤ The process of adding impurity atoms to a pure semiconductor is called doping.

⑥ The impurity atoms added to pure semiconductor are called dopants

⑦

Si	Ge
① Barrier voltage at 25°c is 0.7V	① Barrier voltage at 25°c is 0.3V.
② The forward Vtg drop is 0.7V	② The forward Vtg drop is 0.3V
③ Atomic number is 14.	③ Atomic number is 32
④ It has 14 protons & 14 electrons	④ It has 32 protons & 32 electrons.
⑤ 4 Valence electrons	⑤ 4 Valence electrons
⑥ Resistivity at 20°c is 2500 Ω-M	⑥ Resistivity at 20°c is 0.45 Ω-M

⑦ At room temperature, the intrinsic concentration is $1.5 \times 10^{16}/m^3$	⑦ At room temperature, the intrinsic concentration is $2.5 \times 10^{19}/m^3$
⑧ The maximum temperature rating is about 200°C	⑧ The maximum temperature rating is about 100°C.
⑨ Higher PIV & Current rating compared to Ge	⑨ Lower PIV & Current rating Compared to Si
⑩ Reverse saturation current is less	⑩ Reverse saturation current is high

MODULE-1

SEMICONDUCTOR DIODES AND APPLICATIONS

Syllabus: P-n junction diode, characteristics and parameters. Diode approximations, DC load line analysis. Half wave rectifier, Two-diode Full-wave rectifier, Bridge rectifier. Capacitor filter circuit (only Qualitative approach), Zener diode voltage regulators: Regulator circuit with no load, loaded regulator. Numerical examples as applicable.

Introduction:

Extrinsic semiconductors are classified into

① n-type ② p-type

① n-type:

→ When a small amount of pentavalent impurity is added to a pure semiconductor, it is known as n-type semiconductor.

→ Typical examples of pentavalent impurities are, arsenic (As), antimony (Sb) phosphorus (P), bismuth (Bi) etc

→ Electrons are majority carriers & holes are minority carriers.

② p-type:

→ When a small amount of trivalent impurity is added to a pure semiconductor, it is called p-type semiconductor.

→ Typical examples of trivalent impurities are gallium (Ga), indium (In), aluminium (Al), Boron (B) etc.

→ Holes are majority carriers & electrons are minority carriers.

* **P-n junction: ① Semiconductor diode:**

→ When a P-type Semiconductor is suitably joined to n-type Semiconductor by special fabrication technique, a P-n junction is formed. (Fig ①)

→ P-n junction is called as Semiconductor diode ② P-n junction diode ③ Simply a Crystal diode.

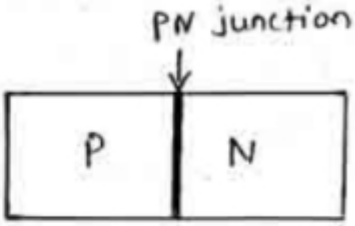
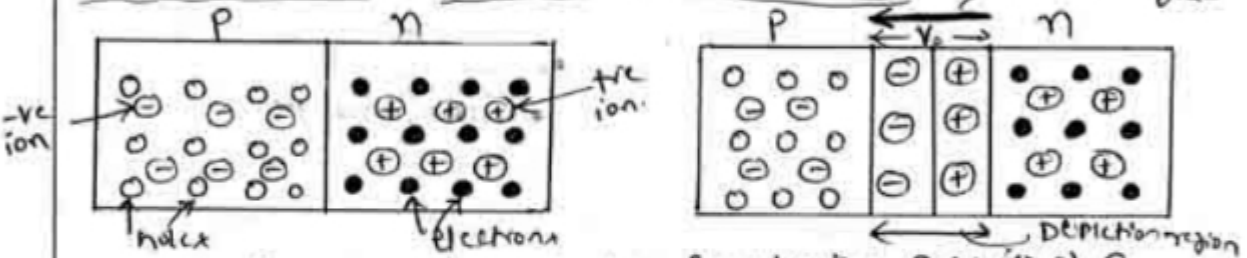


Fig ①: P-n junction

* **Explanation: (Properties of Pn junction) (Formation of depletion layer): (Unbiased Pn junction):**



→ The P-region has holes (majority carriers) & negatively charged impurity atoms, called negative ions (or acceptor ions).

→ The N-region has free electrons (majority carriers) & positively charged impurity atoms, called positive ions (or donor ions).

→ The holes, from the P-region diffuse to the N-region where they combine with the electrons. This creates a layer of negative charges (trivalent ions) near the junction.

→ The free electrons, from the N-region diffuse to the P-region, where they combine with holes. This creates a layer of positive charges (pentavalent ions) near the junction.

→ The region (layers) containing the positive & negative charges in the vicinity of the junction is called

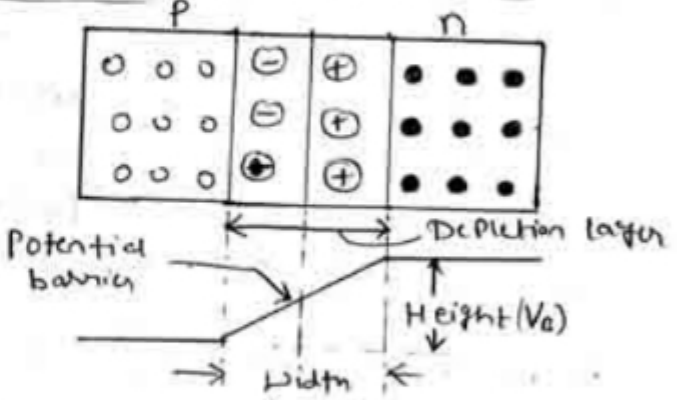
Depletion region (depletion layer) (space charge region) (transition region)

→ The electrons, trying to diffuse into the P-region are repelled by the negative charge of the acceptor ions. Similarly, the holes trying to diffuse into N-region are repelled by the positive charge of the donor ions.

Note:

① Barrier Voltage @ Barrier Potential @ Junction Potential @ Built-in Potential @ Cut-in Potential

→ Once PN junction is formed and depletion layer created, the diffusion of charge carriers stops.



→ The depletion region acts as a barrier to the further movement of charge carriers.

→ The depletion layer behaves like an insulator.

→ The positive & negative charges set up an electric field.

→ The potential difference across the depletion layer is called barrier potential (V_B).

→ V_B = 0.6 V to 0.7V for Si. V_B = 0.2V to 0.3V for Ge.

② Effect of temperature on Barrier Voltage

→ The barrier voltage depends upon ① Density ② Electronic charge & ③ Temperature.

→ For a given pn junction, the first two factors are constant.

→ For both Ge & Si, the value of V_B decreases by 2mV/°C

ie $\Delta V_B = -0.002 \times \Delta t$

where, Δt → Increase in temperature in °C.

→ A pn junction, across which no external voltage source is connected, is known as unbiased PN junction.

③ In an unbiased PN junction, the majority carrier current & minority carrier current are equal in magnitude & flow in opposite direction. Thus there is no net flow of current across the junction.

④ The higher the doping level, the thinner will be the depletion layer and vice versa.

⑤ In 1919, William Henry Eccles coined the term 'diode' from the Greek roots dia means "through" & ode means "path".

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* ⑥ Biasing the pn junction: (Applying DC Voltage across pn junction):

→ Connecting a pn junction to an external DC voltage is called biasing.

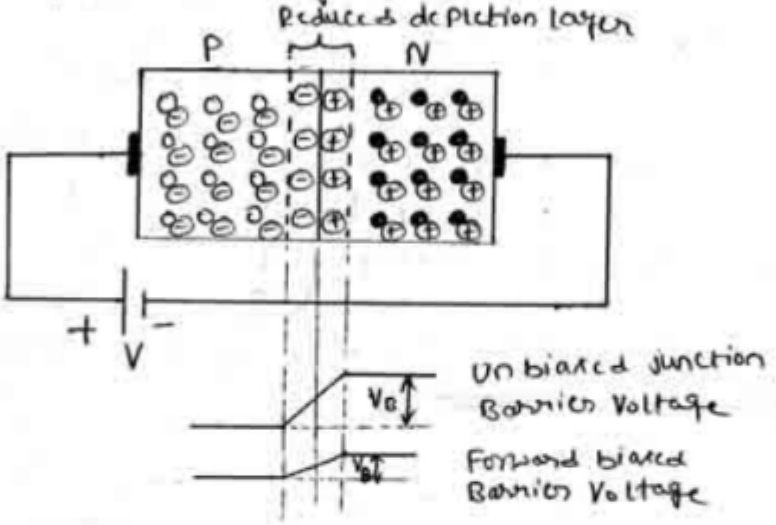
→ The biasing is classified into two types mainly.

① Forward biasing ② Reverse biasing.

① Forward biasing:

When external dc voltage applied to the junction is in such a direction that it cancels the potential barrier, thus permitting current flow, it is called forward biasing. ⑧

A semiconductor diode is said to be forward biased, when the positive terminal of the voltage source is connected to the P-side and negative terminal to the n-side.



Explanation:

→ The holes are repelled by the positive terminal of the voltage source and are forced to move towards the junction.

→ The electrons are repelled by the negative terminal of the voltage source and move towards the junction.

→ Some of the holes and electrons enter the depletion layer and recombine themselves. Thus the width of the depletion layer ✱ and the barrier potential (barrier voltage) reduces.

→ The junction forward resistance reduces and a large current (forward current) flow through the PN junction. (of the order of mA)

Note: ✱ Diffusion ⑧ Storage capacitance:

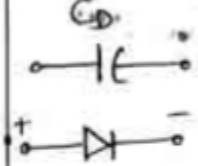
→ The capacitance which exists in a forward-biased junction, is called a diffusion capacitance.

→ Diffusion capacitance is much larger than the transition capacitance (∵ width of the depletion layer is very less). Typical value of C_D is 0.02MF

→ Diffusion capacitance C_D is given by,

$$C_D = \frac{dQ}{dV} = \frac{\tau I_F}{\eta V_T} = \frac{\tau I_F}{V_F}$$

where C_D

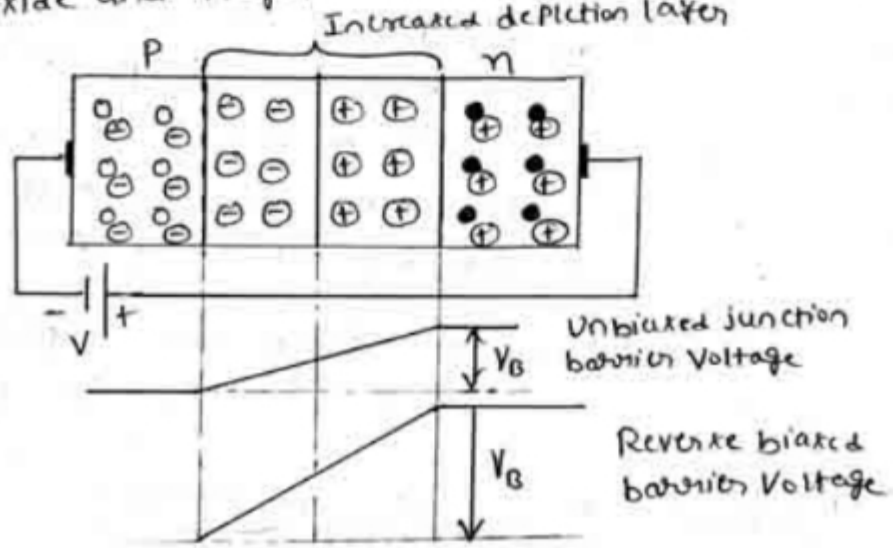


τ → Mean life time of the carriers.
I_F → Value of forward current.
η → A constant ($\eta = 1$ for Ge, $\eta = 2$ for Si)
V_F → Forward voltage
V_T → Volt equivalent of temperature.

② Reverse biasing:

When the external dc voltage applied to the junction is in such a direction that potential barrier is increased, it is called reverse biasing. (or)

A pn junction is said to be reverse biased, when the positive terminal of the voltage source is connected to the n-side and negative terminal to the p-side.



Explanation:

→ The holes in the p-region are attracted towards the negative terminal of the voltage source.

→ The electrons in the n-region are attracted towards the positive terminal of the voltage source.

→ Thus the majority carriers are drawn away from the junction. This widens the depletion layer and increases the barrier potential.

→ The junction reverse resistance becomes very high, and hence no current flows.

→ However, a very small current flows due to minority carriers (of the order of μA@mA). This is called reverse saturation current (I_0)

→ If reverse voltage is increased continuously, the kinetic energy of minority carriers increases & a large reverse current flows. This damages (destroy) the junction(diode) permanently. This is called the reverse breakdown of a diode

→ The reverse breakdown (junction breakdown) causes due to two processes.

1. Zener breakdown:

→ When the Pn-junction is heavily doped, the depletion layer is narrow.

→ When the reverse voltage is increased, the electric field at the junction also increases.

→ This strong electric field breaks the covalent bond, As a result, a large number of minority carriers are generated and a large current flows through the

junction. Such a phenomenon is called Zener effect

2. Avalanche effect: (Avalanche breakdown):

→ If the reverse voltage is increased, the minority carriers acquire a large amount of energy (or momentum).

→ These carriers collide with the atoms and break the covalent bonds and generate additional carriers (electron-hole pairs).

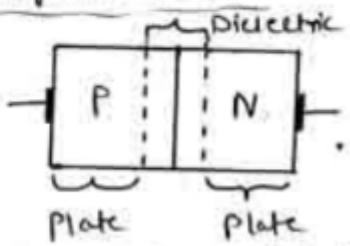
→ These additional carriers pickup energy from the applied voltage and generate still more carriers (carrier generation or carrier multiplication).

→ As a result, the reverse current increases rapidly This process is called Avalanche multiplication or Avalanche effect or Avalanche breakdown.

Note:

① Depletion layer Capacitance ② Simply junction Capacitance
③ Transition Capacitance ④ Space-charge capacitance
⑤ depletion region Capacitance

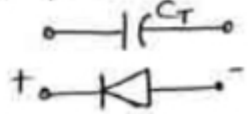
→ P region & N-region act as two plates of a capacitor, seperated by a dielectric (ie depletion layer)



→ The capacitance which exists in a reverse-biased junction is called depletion layer capacitance.

→ The depletion layer capacitance C_T is given by,

$$C_T = \frac{K}{(V_B - V)^n}$$



Where K → A constant, depending upon the semiconductor
V_B → Barrier Voltage

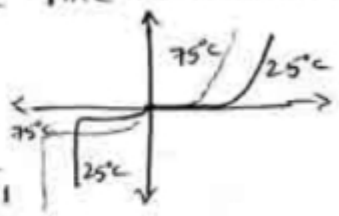
V → Applied reverse voltage
n → A constant depending upon the nature of the junction.

② Junction temperature effects: (Effect of temperature on diode characteristics)

→ The reverse saturation current (leakage current) approximately doubles for each 10°C rise in temperature

→ current at T_2 is,

$$I_o(T_2) = I_o(T_1)\left[2^{(T_2-T_1)/10}\right]$$



Where, $I_o(T_1)$ → reverse current at T_1

③ Diode equation @ diode current equation @ Shockley equation:

The equation relating Pn-junction current & voltage levels is called the Shockley equation.

Shockley equation is,

$$I_D = I_o\left[e^{V_D/\eta V_T} - 1\right] \quad -①$$

Where, I_D → Junction current.
I_o → Reverse saturation current.
V_D → Junction Voltage
η → constant (1 for Ge, & 2 for Si)
V_T → Volt equivalent of temperature = $\frac{KT}{q}$ (Thermal Voltage)

Where
K → Boltzman's const (1.38×10^{-23} J/K)
T → Absolute Temperature (in Kelvin)
q → Electronic charge (1.6×10^{-19} C)

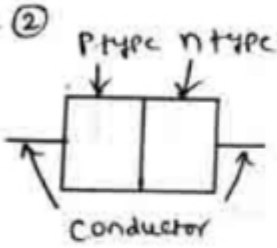
T(Kelvin) = 273 + temp°c

① For an unbiased Pn junction: $V_D = 0$ ∴ $I_D = 0$
② For Forward biased $I_D = I_o e^{V_D/\eta V_T}$
③ For Reverse biased

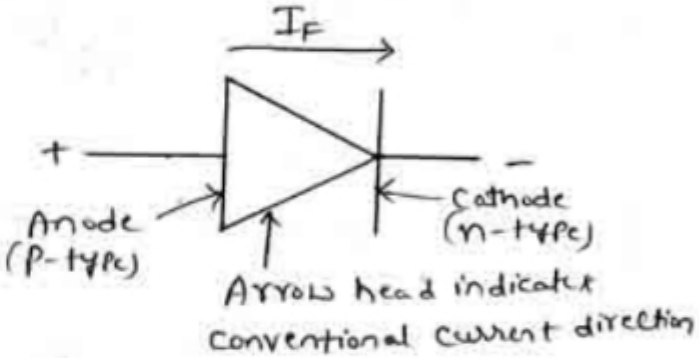
④ PN junction diode:

A PN junction diode is a two terminal unidirectional device, offering a low resistance when forward-biased, and behaving almost as an open switch when reverse biased.

The circuit symbol (or graphic symbol) is shown in fig ②



Fig①: A semiconductor diode



Fig②: Diode circuit symbol

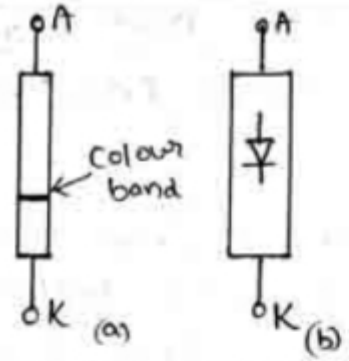
⑤ Types of diodes (Classification of diodes):

Depending upon physical size (or current), diodes are classified into,

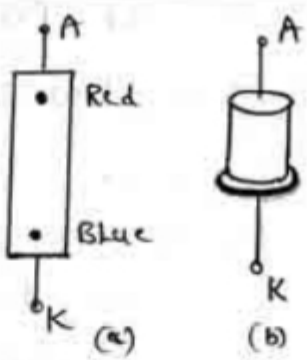
① Low current diodes ② Medium current diodes
③ High current diodes (Power diodes)

① Low current diodes:

→ Low current diodes are 0.3cm long.
→ Colour band is near the cathode (K).
→ Capable of passing a maximum forward current of 100mA.
→ Capable of withstanding 75V reverse voltage (without breaking down)
→ Reverse current is usually less than 1μA (at 25°C)



Fig① : Low current diodes



Fig② : Medium current diode

Fig③ : High current diode

② Medium-current diodes:

→ The end lying near the blue dot is a Cathode, while the other end is anode (fig 2a)

→ The diode is Packaged in a metal can-like casing.

→ The typical diameter is 8.9mm and length is 7.6mm.

→ These diodes are bigger in size Compared to low current diodes.

→ The diodes can pass a forward current of about 400mA and can withstand (survive) reverse Voltage of about 200V.

③ High-current diodes: (Power diodes)

→ These diodes are mechanically connected to a metal heat sink (for the heat dissipation)

→ The typical diameter is 7.8mm and the length is 31.2mm

→ These diodes can pass a forward currents of many amperes and can withstand reverse Voltage of several hundred Volts.

→ These diodes are bigger in size compared to low current & Medium current diodes.

* V-I Characteristics of PN junction (Diode) (or) Forward & reverse Characteristics of PN junction

(1) Forward Characteristics:

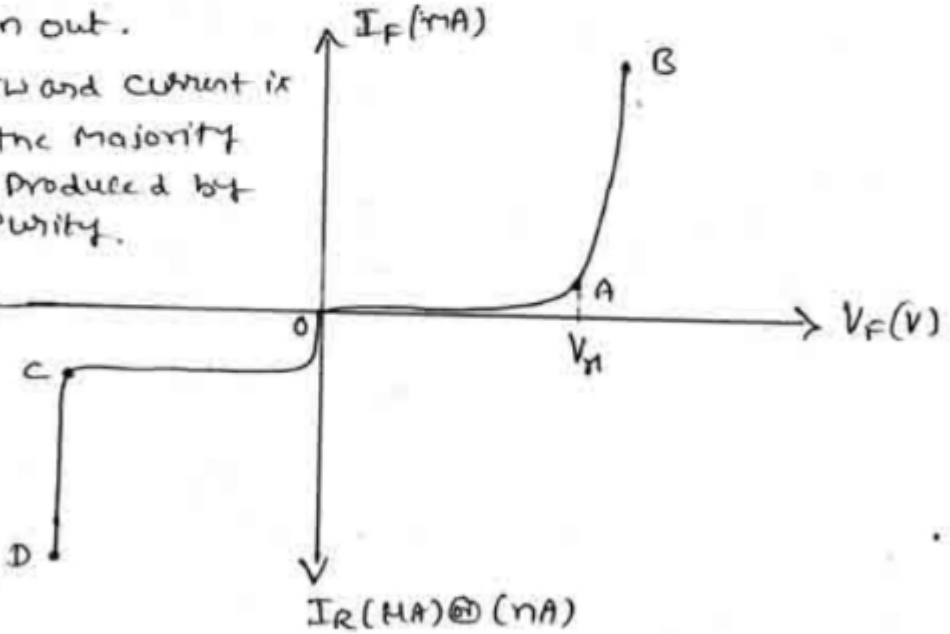
→ P-type is connected to positive terminal & n-type is connected to negative terminal of the battery.

→ A very small forward current (I_F) flows until the forward voltage (V_F) exceeds the cut-in voltage (V_H) (Portion OA)

→ When the forward voltage exceeds the cut-in voltage the current increases rapidly. (Portion AB)

→ The applied voltage should not be increased beyond a certain safe limit, otherwise the diode is likely to burn out.

→ The forward current is due to the majority carriers produced by the impurity.



(2) Reverse Characteristics:

→ P-type is connected to negative terminal & n-type is connected to positive terminal of the battery.

→ When the applied reverse voltage (V_R) is below the breakdown voltage (V_{BR}), the diode current is very

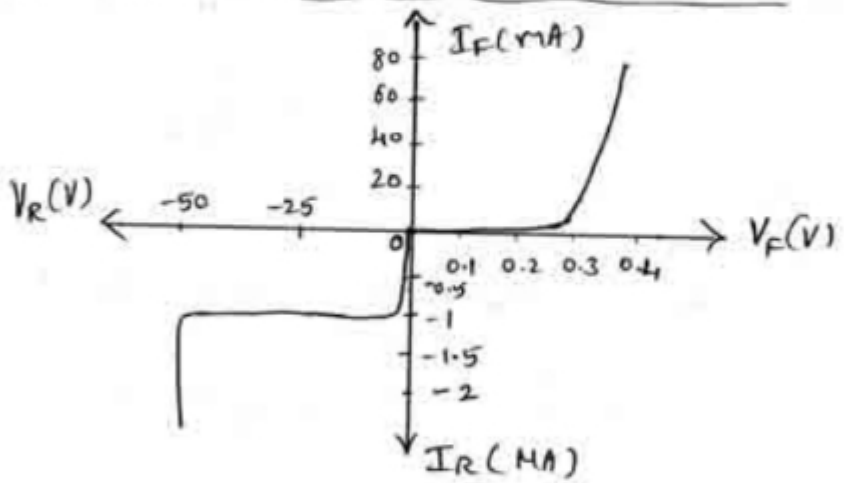
small and remains constant. This value of current is called reverse saturation current (I_0). (Region OC)

→ When the reverse voltage exceeds breakdown voltage, the current increases very rapidly. (Region CD)

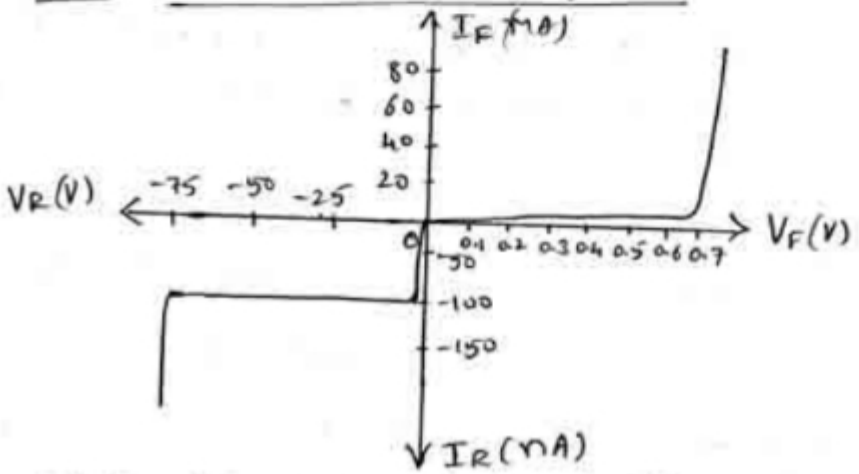
→ The applied voltage should not be increased beyond the breakdown voltage, otherwise the diode is destroyed permanently.

→ The reverse current is due to the minority carriers produced due to breaking of some covalent bonds.

Note: ① V-I characteristics of Ge & Si



Fig①: VI characteristics of Ge



Fig②: VI characteristics of Si

Ge (Fig 1)
Forward Characteristics:

→ A very small forward current flows until the forward voltage exceeds 0.3V.

→ When the forward voltage exceeds 0.3V, the current increases rapidly.

Reverse characteristics:

→ When the applied reverse voltage is below the breakdown voltage, the diode current is very small, typically around 1 μA. (which is larger than the reverse current for a Silicon diode)

→ When the reverse voltage exceeds breakdown voltage, (around 50V), the current increases very rapidly.

→ Reverse breakdown voltage for Ge is less than that of Si

→ From the characteristics, $|I_F| >> |I_R|$

Si (Fig 2)
Forward Characteristics:

→ A very small forward current flows until the forward voltage exceeds 0.7V.

→ When the forward voltage exceeds 0.7V, the current increases rapidly.

Reverse characteristics:

→ When the applied reverse voltage is below the breakdown Voltage, the diode current is very small, typically around (100 nA).

→ When the reverse voltage exceeds breakdown voltage (around 75V), the current increases very rapidly.

→ From the characteristics, $|I_F| >> |I_R|$.

② Conditions under which a PN junction can be destroyed

(i) Pn junction diode is over heated by a high forward current. [$I_{F(max)}$]

(ii) A large reverse voltage causes the Pn junction to break down. [$V_{R(max)}$]

Diode Parameters (Important terms):

(i) Forward voltage (or) (Knee voltage) (or) (Forward voltage drop) (or) turn-on voltage (or) Potential barrier voltage: (V_γ):

→ It is the voltage applied across a forward biased device. (or)

The forward voltage is the voltage at which the current through the junction starts to increase rapidly.

→ The knee voltage for Si diode is 0.7V and 0.3V for Ge diode

(ii) Maximum forward current: ($I_{F(max)}$):

→ It is the maximum current that a diode can withstand under forward bias condition, without permanent damage to the Pn junction due to over heating

(iii) Forward current: (I_F):

→ It is the current flowing through a forward biased diode.

(iv) Reverse breakdown voltage (or) Breakdown voltage: (V_{BR}):

It is the reverse voltage at which the Pn junction diode breaks down and reverse current increases rapidly (permanently damages the diode) (or)

It is the minimum reverse voltage at which Pn junction breaks down with sudden rise in reverse current.

→ The reverse breakdown voltage is around 50V for Ge diodes and 75V for Si diodes.

(v) Reverse Voltage: (V_R)

→ It is the voltage across a reverse biased diode.

(vi) Reverse Current: (Reverse bias current): (I_R) (Leakage current)

→ It is the direct current flowing through a reverse-biased diode. This current is due to the minority carriers

(vii) Reverse Saturation Current: (I_o)

→ It is the nominal current, which flows through the diode when it is reverse biased. (or)

It is the constant reverse current flowing through the reverse biased diode.

→ It is in the order of μA for Ge diodes and nA for Si diodes.

(viii) Peak inverse Voltage: (PIV)

→ It is the maximum reverse voltage that a diode can withstand without destroying the junction.

→ There are two types of PIV

(i) Repetitive PIV (ii) Non-repetitive PIV

→ PIV may be between 10V and 10kV depending upon the type of diode.

(ix) Power dissipation (P_D):

The power dissipated in a diode for a given value of diode voltage (V_D) and current (I_D)

i.e. $P_D = V_D \times I_D$

(X) Maximum power rating @ Maximum power dissipation rating ($P_{D(max)}$):

It is the maximum power that can be dissipated at the junction without damaging it.

Maximum power rating is given by,

$$P_{D(max)} = V_{D(max)} \times I_{D(max)}$$

(Xi) Maximum junction temperature (T_J):

It is the maximum allowable junction temperature of the diode.

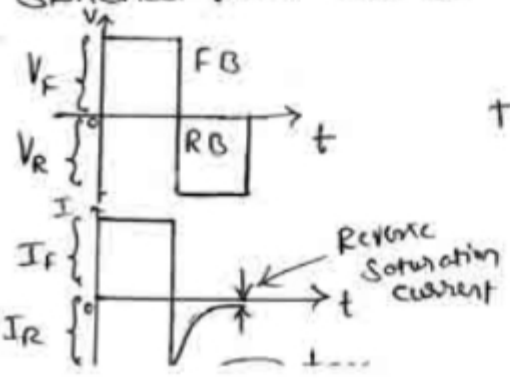
(Xii) Forward recovery time (t_{fr}):

It is the time required for the forward current @ voltage to reach a specified value after the diode has been abruptly switched from the reverse-biased state to the forward-biased state.

(Xiii) Reverse recovery time (t_{rr}):

It is the time required by the reverse current @ voltage to reach a specified value, when the diode is switched from the forward-biased condition to the reverse-biased condition abruptly.

@ It is the time required for the current to decrease to the reverse saturation current level, when the diode is switched from the forward-bias to reverse bias.



The minimum fall time of the applied voltage pulse is,

$$t_{f(min)} = 10 t_{rr}$$

Note:

① The maximum power dissipation (W)

$$P_2 = (P_1 \text{ at } T_1) - (D \times \Delta T)$$

Where,
P_1 (or) → power at temp T_1 (W)
D → Derating factor (W/°C)
ΔT → temperature change (°C) $(T_2 - T_1)$
T_1 → Temperature (°C)

② The diode forward voltage drop is, (at any temperature)

$$V_{F_2} = (V_{F_1} \text{ at } T_1) + [\Delta T \ (\Delta V_F / °C)]$$

Where,
V_{F_1} → Forward Vtg drop at T_1 (V)
$\Delta T \rightarrow (T_2 - T_1)$ → Temperature change (°C)
$\Delta V_F/°C$ → Voltage / Temperature coefficient. (V/°C)
= −1.8 mV/°C for Si, −2.02 mV/°C for Ge

③ Dynamic resistance of a forward-biased diode at any temperature is,

$$r_d' = \frac{26\text{ mV}}{I_F}\left(\frac{T + 273°C}{298°C}\right)$$

Where, I_F → Forward current (A)
T → Junction temperature (°C)

---

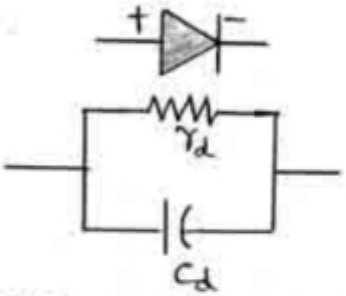
* Equivalent circuits: (Models): ⑤ (Diode Models)

An equivalent circuit for a device is a circuit that represents the device behavior under forward and reverse bias conditions.

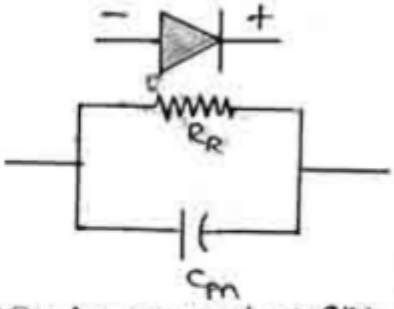
① AC equivalent circuits:

A forward-biased diode can be represented by the dynamic resistance 'r_d' in parallel with the diffusion capacitance 'C_d (C_D)' [Fig(1)]

A reverse-biased diode can be represented by the high reverse resistance 'R_R' in parallel with the depletion layer capacitance 'C_{TH} (C_T)' [Fig(2)]

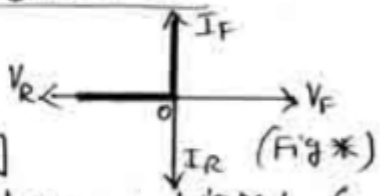


Fig①: AC equivalent ckt for a forward-biased diode



Fig②: AC equivalent ckt for a reverse-biased diode

② DC equivalent circuits:



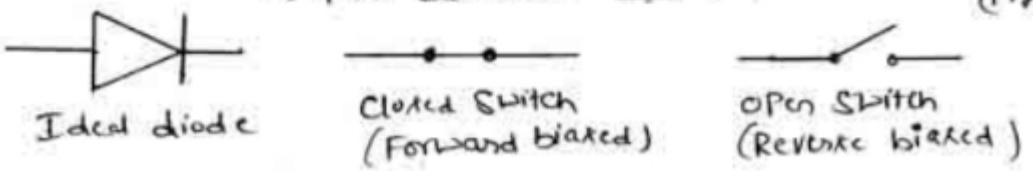
(Fig*)

(i) Ideal diode equivalent ckt: [Fig(3)]

→ The diode conducts when it is forward biased & has zero resistance (acts as closed switch)

→ The diode blocks the conduction when it is reverse biased and has infinite resistance (acts as open switch)

→ This equivalent ckt has ideal characteristic (Fig*)

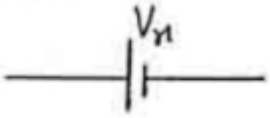


Fig③: Ideal diode equivalent circuit

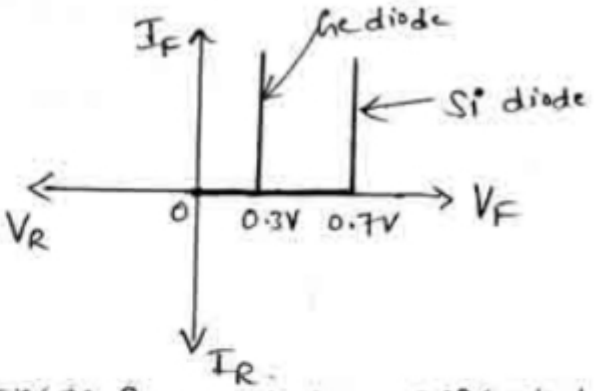
(ii) Non ideal diode equivalent circuit (Practical diode) (Fig 4)

Approximate equivalent circuit ⓐ Basic dc equivalent circuit

The diode equivalent circuit consists of a voltage source with a voltage V_γ and negligible forward resistance. This equivalent circuit has the second approximation characteristics (or Approximate characteristics) shown in fig ⑤.



Fig(4): Basic dc equivalent circuit



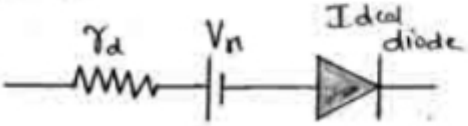
Fig(5): Ge & Si diode approximate characteristics

(iii) Piecewise linear equivalent circuit: (Complete DC equivalent circuit) (Third approximation equivalent ckt) (Fig 6)

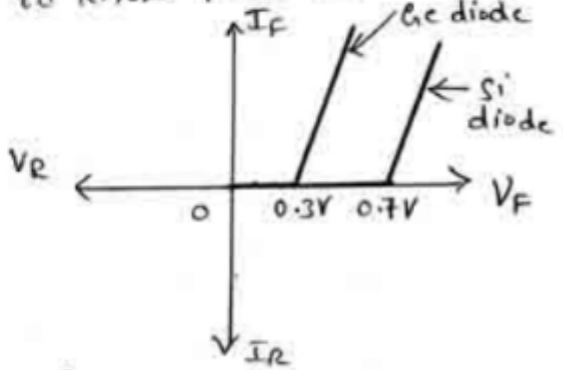
The equivalent circuit consists of diode dynamic resistance 'r_d' in series with the voltage source V_γ.

This equivalent circuit has the piecewise linear characteristics shown in fig ⑦.

An ideal diode is included to show that current flow only in one direction.



Fig(6): Complete dc equivalent circuit



Fig⑦: Ge & Si diode piecewise linear characteristics

* Diode approximations:

There are three diode approximations, namely

① Ideal diode approximations :

→ An ideal diode (Perfect diode) have Zero forward resistance and infinite reverse resistance (Zero forward voltage drop @ cut-in Voltage)

→ A forward biased diode can be replaced by a short circuit (SC) and reverse biased diode can be replaced by a open circuit (OC)

→ Fig ① shows the ideal diode characteristics.

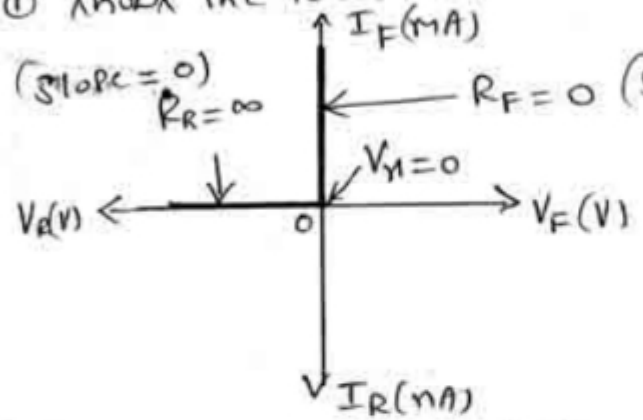


Fig ①: Ideal diode characteristics

(a) Short circuit (Closed switch)
Forward biased

(b) Open circuit (Open switch)
Reverse biased

② Near-ideal diode approximation (a) (Second approximation) (b) (Practical approximation) (c) (Approximate characteristics)

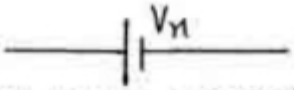
(Simplified equivalent approximation)

→ An ideal diode doesn't exist practically, there are many applications where diodes can be assumed to be near-ideal diodes.

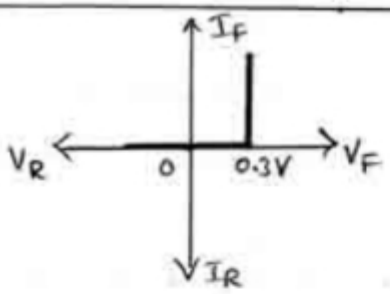
→ The cut-in voltage is 0.3V for Ge & 0.7V for Si

→ The reverse current is very small so it can be ignored

→ Fig ② shows the approximate diode characteristics

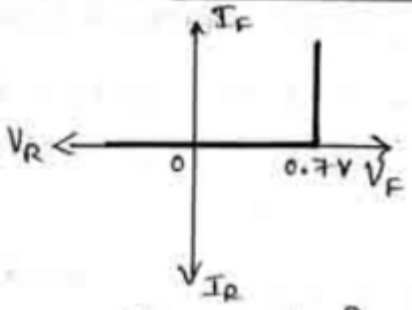


Simplified equivalent circuit



$V_{\gamma} = 0.3V$, $R_F = 0$, $R_R = \infty$,
$I_R = 0$

Fig: Approximate characteristics of the diode



$V_{\gamma} = 0.7V$, $R_F = 0$, $R_R = \infty$
$I_R = 0$

Fig: Approximate characteristics of Si diode

Fig ②: Approximate Characteristics

③ Piecewise linear approximations:

→ When the forward characteristic of a diode is not available, a straight line approximation called the piecewise linear approximation is used.

→ Construction of piecewise linear characteristic

Step 1: Mark $V_F (V_{\gamma})$ on X-axis. [Point $A(V_F, 0)$]

Step 2: Draw a straight line (Let AB) with a slope equal to the reciprocal of the dynamic resistance of the diode.

→ It consists of two straight line pieces, one horizontal and other with slope $1/\gamma_d$

→ Fig ② shows the piecewise linear characteristics

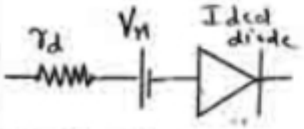


Fig: Simplified Equivalent circuit

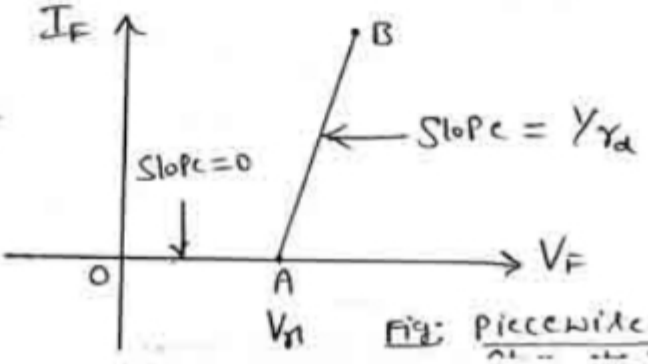


Fig: Piecewise Linear

* Resistance of diode:

① DC (or) Static resistance:

It is the opposition offered by the diode to the direct current.

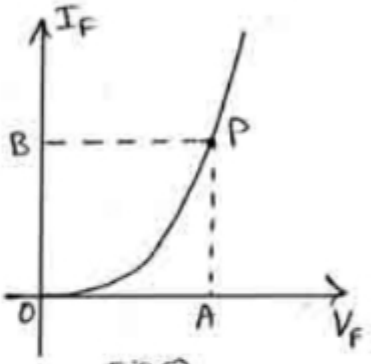
② Static forward resistance (or) DC forward resistance:

→ It is the opposition offered by the forward biased diode to the direct current, denoted by R_F (or) R_f.

→ It is measured by the ratio of d.c. voltage across the diode to the resulting d.c. current through it.

→ From the forward characteristics of fig①, the dc forward resistance at P is,

$$R_F = \frac{\text{Forward d.c. Voltage}}{\text{Forward d.c current}} = \frac{OA}{OB}$$



Fig①

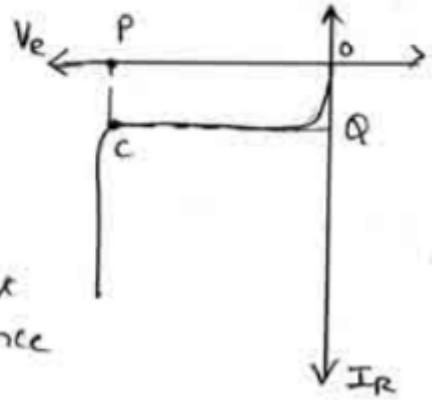
③ Static reverse resistance (or) DC reverse resistance:

→ It is the opposition offered by the reverse biased diode to the direct current, denoted by R_R (or) R_r.

→ It is measured by the ratio of reverse d.c. voltage across the diode to the reverse saturation current.

→ From the reverse characteristics of fig②, the dc reverse resistance at C is,

$$R_R = \frac{\text{Reverse d.c. Voltage}}{\text{Reverse Saturation current}} = \frac{OP}{OQ}$$



Fig②

(2) AC (or) Dynamic (or) Incremental resistance:

→ It is the opposition offered by the forward biased diode under a.c conditions (when the applied voltage is a.c) (or)

It is the reciprocal of the slope of the forward characteristics beyond its knee, denoted by r_d (or) r_F (or) r_f

→ It is measured by the ratio of change in applied voltage to the change in the current.

→ From the forward characteristics of fig (3), the dynamic forward resistance is,

$$r_d = \frac{\Delta V_F}{\Delta I_F} = \frac{1}{\text{Slope of forward characteristics}}$$

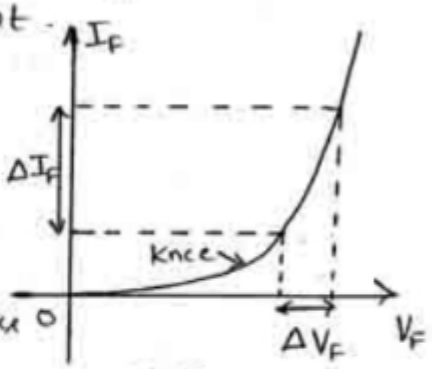


Fig (3)

→ r_d includes dc resistance of the semiconductor material. The pure ac resistance is given by,

$$r_d' = \frac{0.026}{I_F} \quad -(*)$$

Where, I_F → DC forward current

Eqn (*) is valid at 25°c only.

→ Semiconductor substrate resistance is,

$$r_{substrate} = r_d - r_d'$$

* DC load line:

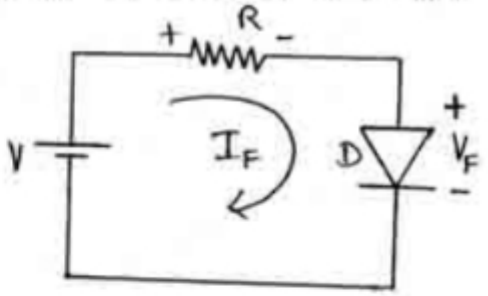
A DC load line is a straight line on the diode characteristic which describes all the dc conditions that exist within the circuit.

Explanation:

The graphical analysis used to calculate the precise [illegible] and voltage is called dc load

line analysis.

Consider a simple diode circuit as shown in fig①.



Fig① : Simple diode circuit

→ The diode is forward biased, so the diode forward current I_F flows through resistor 'R'.

→ Applying KVL to the ckt, we get

$$V - I_F R - V_F = 0$$

$$\Rightarrow \quad V = I_F R + V_F \quad -(*)$$

Put $I_F = 0$ in eqn (*)

$$V = V_F$$

or $\boxed{V_F = V}$

Now mark point A(V, 0)

Put $V_F = 0$ in eqn(*)

$$V = I_F R$$

$$\Rightarrow \boxed{I_F = \frac{V}{R}}$$

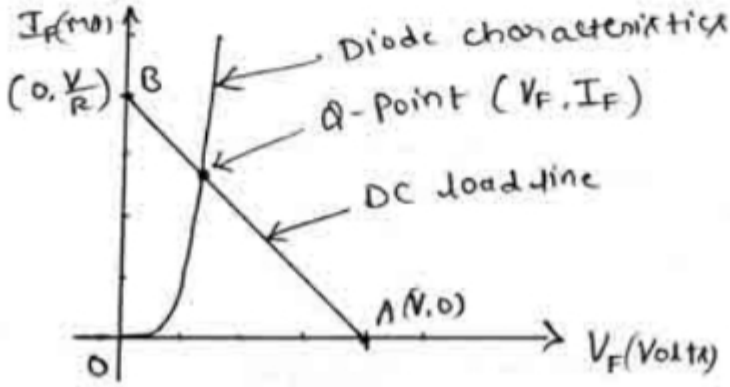
Now mark point $B(0, \frac{V}{R})$

Joint AB to get the dc load line

From eqn (*), we can write

$$V - V_F = I_F R$$

$$\Rightarrow I_F = \left(\frac{-1}{R}\right) V_F + \frac{V}{R} \quad -(**)$$



Q- Point (or) Quiescent Point (or) dc bias Point (or) operating Point (or) Working bias Point:

→ The intersection of the diode forward characteristic and the dc load line is called the Q-Point.

→ The values of forward current through the diode (I_F) and the voltage drop across the diode (V_F) can be found at Q-Point.

Note:

① To Calculate the load resistance (R) and Supply Voltage (V)

Consider eqn (**).

$$I_F = \left(\frac{-1}{R}\right)V_F + \frac{V}{R}$$

This equation is of the form $y = mx + c$

where, $y = I_F$, $m = -\frac{1}{R}$, $x = V_F$, $c = \frac{V}{R}$

① Given Q-Point and Supply Voltage (V):

→ Load line is drawn from Point A $(V, 0)$ through Q-Point.

→ Load resistance 'R' is calculated from the slope of the load line.

② Given Q-Point and load resistance (R):

→ Load line is drawn through Q-Point and having slope $1/R$.

→ The intersection of the load line with x-axis gives the value of Supply Voltage (V).

② Transformer utilization factor (T.U.F)

$$T.U.F = \frac{\text{D.C Power delivered to the load}}{\text{A.C rating of the transformer}}$$

For HWR, T.U.F = 0.287
For FWCTR, T.U.F = 0.693
For FWBR, T.U.F = 0.812

* Rectifier:

A circuit (device) which converts a.c. voltage into pulsating d.c. voltage is called rectifier.

The different types of rectifier circuits are

(i) Half-Wave rectifier

(ii) Full-Wave rectifier

(a) Centre tapped full wave rectifier

(b) Bridge full wave rectifier

(a) Half-Wave rectifier: (HWR):

Definition: The rectifier which conducts current (Voltage) only during one half-cycle of the ac input is called Half-Wave rectifier.

Circuit diagram and input & output wave forms:

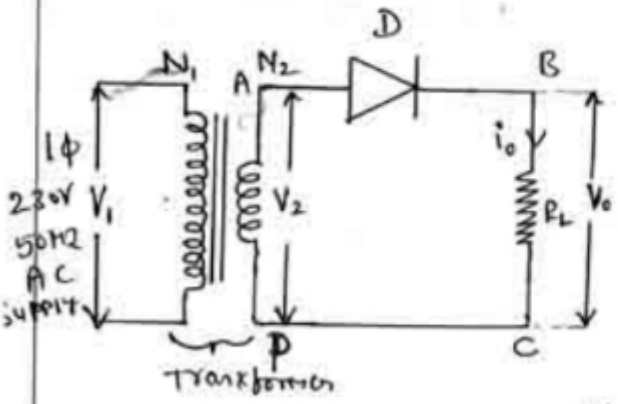
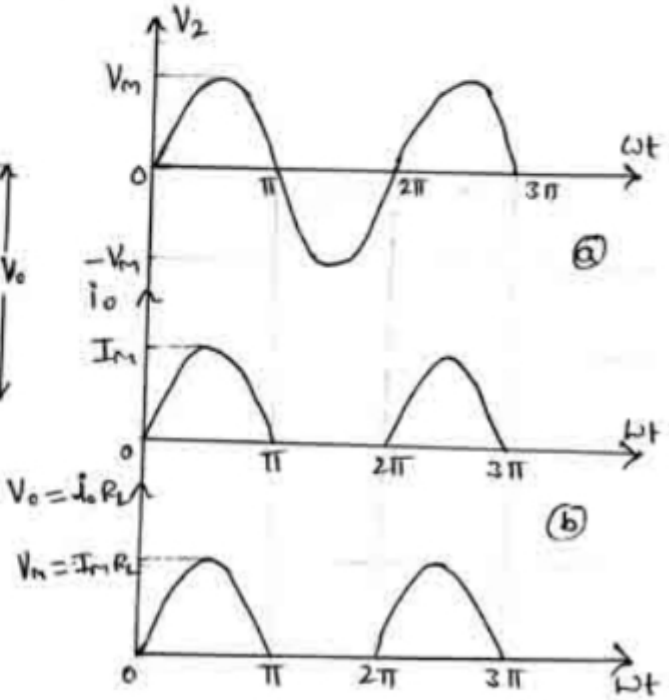


Fig: Half wave rectifier



(a) Waveform of secondary transformer voltage

(b) Load current waveform

(c) Load voltage waveform

Construction: It consists of a step down transformer, a diode and a load resistor. The primary coil of a transformer is connected to ac input and secondary coil to a load resistor (R_L) through the diode (D).

Operation: (Principle of operation):

→ During positive half cycle of the input voltage, end A becomes positive w.r.t end P. Hence the diode is forward biased and current flows through R_L (Path: ADBCPA). $[V_o = i_o R_L]$

→ During negative half cycle of the input voltage, end A becomes negative w.r.t end P. Hence the diode is reverse biased and no current flows in the circuit. $[V_o = 0]$

Therefore, current flows through the diode during positive half-cycles of input a.c. voltage only, it is blocked during the negative half-cycles.

Note:

① **Uses of transformer:**

(i) It allows us to step up or step down the a.c input voltage.
(ii) It isolates the rectifier circuit from power line and thus reduces the risk of electric shock.

② **Disadvantages or Drawbacks of HWR:** or **Demerits**

(i) The ripple factor is too high ($\gamma = 1.21$)
(ii) Efficiency of rectification is low ($\eta = 0.406$)
(iii) The T.U.F (Transformer utilization factor) is very low.
(iv) D.C. Saturation of transformer secondary winding takes place.

~~**Advantages or Merits of HWR**~~:

(v) The a.c supply delivers power only half the time. Therefore, the output is low.

(vi) An additional filtering is required to produce steady

direct current (Pulsating current in the load contains alternating component whose basic frequency equal to the supply frequency).

⑤ Advantages & Merits of HWR:

(i) only one diode is required
(ii) No centre-tap on the transformer is required.

⑥ Current through diode & R_L & Peak load current ($\dot{I}_o$) & Peak diode current (I_m)

$V_m >> I_m$

Instantaneous supply voltage is,

$$V_1 = V_m \sin \omega t \quad -①$$

Instantaneous secondary voltage is,

$$V_2 = \frac{N_2}{N_1} V_1 \quad -②$$

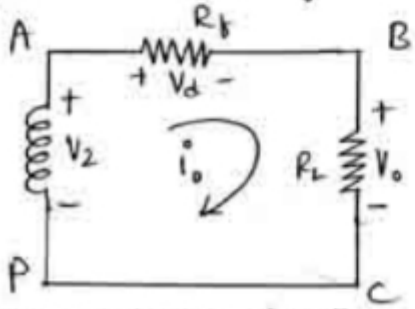
Using ① in ②, we get

$$V_2 = \frac{N_2}{N_1} V_m \sin \omega t$$

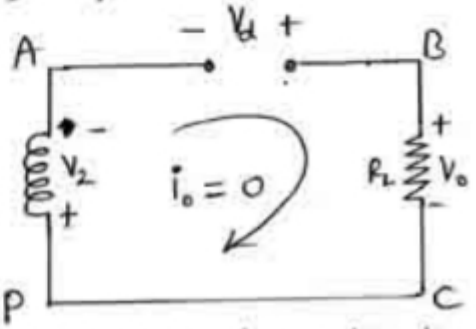
Let $N_1 = N_2$, then

$$V_2 = V_m \sin \omega t \quad -③$$

The equivalent circuit when the diode is conducting & not conducting is shown below,



Fig① Equivalent circuit when diode is conducting



Fig② Equivalent circuit when diode is not conducting

Where

$R_f \rightarrow$ Forward resistance of the diode.

From fig ①

$$i_o = \frac{V_2}{R_f + R_L} \; ; \; 0 \le \omega t \le \pi \quad \text{—④}$$

Using ② in ④, we get

$$i_o = \frac{V_M \sin \omega t}{R_f + R_L} \; ; \; 0 \le \omega t \le \pi$$

$$i_o = I_m \sin \omega t \; ; \; 0 \le \omega t \le \pi \quad \text{—⑥}$$

where $I_m = \frac{V_M}{R_f + R_L}$

From fig ②

$$i_o = 0 \; ; \; \pi \le \omega t \le 2\pi \quad \text{—⑤}$$

From ⑤ & ⑥, we can write

$$i_o = \begin{cases} I_m \sin \omega t & ; \; 0 \le \omega t \le \pi \\ 0 & ; \; \pi \le \omega t \le 2\pi \end{cases} \quad \text{—⑦}$$

→ current through diode & R_L

where, $I_m = \frac{V_M}{R_f + R_L}$ —⑧

→ Peak load current & Peak diode current

Derivations:

① Average load current (or) DC load current (or) DC output current & Average output current (I_{dc}):

DC load current,

$$I_{dc} = \frac{\text{Area under one cycle of } i_o}{\text{Period of } i_o}$$

$$= \frac{\int_0^{2\pi} i_o \, d\omega t}{2\pi}$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} I_m \sin \omega t \, d\omega t + \cancel{\int_{\pi}^{2\pi} 0 \, d\omega t}^{\,0}\right] \quad \text{(Using 7)}$$

$$= \frac{I_m}{2\pi}\left[-\cos \omega t\right]_0^{\pi}$$

$$= \frac{I_m}{2\pi}[-\cos\pi + \cos 0]$$

$$\boxed{I_{dc} = \frac{I_m}{\pi} \text{ or } 0.3183 I_m} \quad -(9) \quad (\because \cos\pi = -1,\ \cos 0 = 1)$$

(2) Average Load Voltage or DC load voltage or DC output voltage or Average output voltage (V_{dc}):

DC load voltage,

$$V_{dc} = I_{dc} \cdot R_L$$

$$= \frac{I_m}{\pi} \cdot R_L \qquad (\text{using } 9)$$

$$= \frac{1}{\pi}\left[\frac{V_m}{R_f + R_L}\right] R_L \qquad (\text{using } 8)$$

$$\boxed{V_{dc} = \frac{V_m/\pi}{1 + R_f/R_L}} \quad -(10)$$

If diode is ideal, $R_f = 0$

$$\therefore \boxed{V_{dc} = \frac{V_m}{\pi}} \quad -(11)$$

(3) RMS load current (I_{rms}):

RMS load current,

$$I_{rms} = \sqrt{\frac{\text{Area under one cycle of } i_o^2}{\text{Period of } i_o}}$$

$$= \sqrt{\frac{\int_0^{2\pi} i_o^2 \, d\omega t}{2\pi}}$$

$$= \sqrt{\frac{1}{2\pi}\left[\int_0^{\pi} I_m^2 \sin^2\omega t \, d\omega t + \int_{\pi}^{2\pi} 0 \, d\omega t\right]} \qquad (\text{using } 7)$$

$$= \sqrt{\frac{I_m^2}{2\pi}\int_0^{\pi}\left(\frac{1-\cos 2\omega t}{2}\right) d\omega t} \qquad \left(\because \sin^2\theta = \frac{1-\cos 2\theta}{2}\right)$$

$$= \frac{I_m}{2}\sqrt{\frac{1}{\pi}\left\{(\omega t)_0^{\pi} - \left(\frac{\sin 2\omega t}{2}\right)_0^{\pi}\right\}} \quad [\because \sin n\pi = 0,\ n \in I]$$

$$= \frac{I_m}{2}\sqrt{\frac{1}{\pi}(\pi - 0)}$$

$$\boxed{I_{rms} = \frac{I_m}{2}} \quad -(12)$$

④ RMS load voltage (V_{rms})

RMS load voltage.

$$V_{rms} = I_{rms} R_L$$

$$= \left(\frac{I_m}{2}\right) R_L$$

$$= \frac{1}{2}\left(\frac{V_m}{R_f + R_L}\right) R_L$$

$$\boxed{V_{rms} = \frac{V_m/2}{1 + R_f/R_L}} \quad -(13)$$

If diode is ideal, $R_f = 0$

$$\therefore \boxed{V_{rms} = \frac{V_m}{2}} \quad -(14)$$

⑤ Ripple factor (γ):

Ripple factor.

$$\gamma = \frac{V_{ac}}{V_{dc}} \quad -(5)$$

$$= \frac{\sqrt{V_{rms}^2 - V_{dc}^2}}{V_{dc}} \quad [\because V_{rms}^2 = V_{ac}^2 + V_{dc}^2]$$

$$= \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{V_m/2}{1 + R_f/R_L}\right)^2 \Big/ \left(\frac{V_m/\pi}{1 + R_f/R_L}\right)^2 - 1} \quad (\text{using } (10) \text{ \& } (13))$$

$$\gamma = \sqrt{\frac{\pi^2}{4} - 1}$$

$$\boxed{\gamma = 1.21 \text{ (or) } 121\%} \quad -(16)$$

Note:

(1) AC Components present in the dc output of a rectifier are called ripples.

(2) A measure of the smoothness of the dc output of a rectifier is called the ripple factor

(or)

The ratio of rms value of ac component present in the rectified output to the dc component in the rectified output is called ripple factor

$$\text{i.e } \gamma = \frac{V_{ac}}{V_{dc}} \text{ (or) } \frac{I_{ac}}{I_{dc}}$$

(3) We have

$$\left(\begin{matrix}\text{Total RMS value of} \\ \text{rectified output}\end{matrix}\right)^2 = (\text{DC value})^2 + \left(\begin{matrix}\text{RMS value of} \\ \text{ac component}\end{matrix}\right)^2$$

i.e

(or)

$$I_{rms}^2 = I_{dc}^2 + I_{ac}^2 \quad -(17)$$

$$V_{rms}^2 = V_{dc}^2 + V_{ac}^2 \quad -(18)$$

(4) From (15) & (16), we can write

$$\gamma = \frac{V_{ac}}{V_{dc}} = 121\% \implies \boxed{V_{ac} = 121\% \text{ of } V_{dc}} \quad -(19)$$

∴ AC (or) ripple component is 121% of the dc component. Hence HWR is not recommended for practical applications.

---

5) Efficiency (or) Rectification efficiency: (η) (Power conversion efficiency)

Efficiency, $\eta = \frac{P_{dc}}{P_{ac}} \quad -(20)$

$$= \frac{I_{dc}^2 R_L}{I_{rms}^2 (R_f + R_L)} \qquad \left[\because P_{dc} = I_{dc}^2 R_L \;\&\; P_{ac} = I_{rms}^2 (R_f + R_L) \right]$$

$$= \frac{(I_m/\pi)^2 R_L}{(I_m/2)^2 (R_f + R_L)} \qquad [\text{Using (9) \& (12)}]$$

$$= \frac{4}{\pi^2} \frac{R_L}{R_f + R_L}$$

$$\boxed{\eta = \frac{0.406}{1 + R_f/R_L} \text{ or } \frac{40.6\%}{1 + R_f/R_L}} \quad -(21)$$

If diode is ideal, $R_f = 0$

$$\therefore \boxed{\eta = 0.406 \text{ or } 40.6\%} \quad -(22)$$

Note:

① The ratio of the dc output power to ac input power supplied to the rectifier is known as rectification efficiency.

② From (20) & (22), we can write

$$\eta = \frac{P_{dc}}{P_{ac}} = 40.6\% \Rightarrow \boxed{P_{dc} = 40.6\% \text{ of } P_{ac}} \quad -(23)$$

∴ The dc output power is 40.6% of the ac input power (a maximum of 40.6% of a.c input power is converted into dc output power). Hence HWR has a very poor rectification efficiency.

③ The process of converting a.c voltage into pulsating d.c voltage is called rectification.

---

④ Percentage regulation or (Voltage regulation) (% Regulation)

$$\% \text{ Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 \quad -(24)$$

$$= \frac{\frac{V_m}{\pi} - \left(\frac{V_m}{\pi}\right)\frac{R_L}{R_f+R_L}}{\left(\frac{V_m}{\pi}\right)\frac{R_L}{R_f+R_L}} \times 100$$

$$= \frac{1 - \frac{R_L}{R_f+R_L}}{\frac{R_L}{R_f+R_L}} \times 100 \qquad \left[\because V_{NL} = \frac{V_m}{\pi},\ V_{FL} = \left(\frac{V_m}{\pi}\right)\frac{R_L}{R_f+R_L}\right]$$

$$= \frac{\frac{R_f + R_L - R_L}{R_f+R_L}}{\frac{R_L}{R_f+R_L}} \times 100$$

$$\boxed{\%\ \text{Regulation} = \frac{R_f}{R_L} \times 100} \quad — (25)$$

If diode is ideal, $R_f = 0$

$$\therefore \boxed{\%\ \text{Regulation} = 0} \quad — (26)$$

Note: ① From (26), For an ideal diode, a HWR behaves as an ideal dc Power Supply.

② V_{NL} → DC output Voltage when load current is Zero
(or) DC output Voltage when no load

V_{FL} → DC output Voltage with load current
(or) DC output Voltage with load

③ The Variation of dc o/p Voltage as a function of DC load current is called regulation
(or)
The Variation of dc output Voltage as load changes from no load to full load is called regulation

④ Ideally, the dc voltage (O/P) is independent of load current.

$\therefore V_{NL} = V_{FL}$

Hence, % Regulation = 0

⑤ Lesser the value of the voltage regulation, better is the performance of the rectifier circuit.

⑥ $V_{NL} = V_{dc}\Big|_{R_L=\infty} = \frac{V_m/\pi}{1+R_f/\infty} = \frac{V_m}{\pi}$ → (From 10)

$V_{FL} = V_{dc} = \frac{V_m/\pi}{1+\frac{R_f}{R_L}} = \left(\frac{V_m}{\pi}\right)\frac{R_L}{R_f+R_L}$ → $\left(\frac{\text{Anything}}{\infty} = 0\right)$

⑦ $f_{out} = f_{in}$

(Freq of HWR o/p) = (I/P frequency)

---

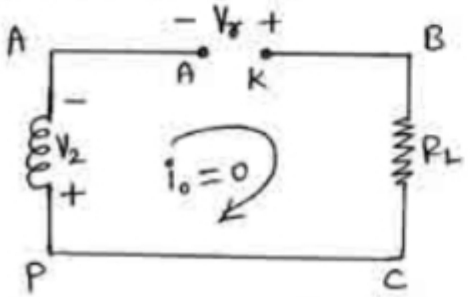
⑧ Peak inverse voltage (or) (Peak reverse voltage) (PIV)

The Peak inverse voltage is the maximum voltage across the reverse biased diode of a rectifier.

(or)

The peak inverse voltage is the maximum reverse voltage to which the diode can be subjected.

The equivalent circuit of a HWR when diode is reverse biased (not conducting) is shown below.



Applying KVL to the loop,

$-V_2 + V_r - i_o R_L = 0$

$\Rightarrow V_r = V_2 \quad (\because i_o = 0)$

$\Rightarrow V_r = V_m \sin \omega t \quad (\because V_2 = V_m \sin \omega t$

$\Rightarrow \boxed{V_{r\max} = V_m = PIV}$ — (27)

$\therefore$ PIV for a HWR is equal to the peak secondary voltage of the transformer.

(ii) Full-Wave rectifier: (FWR):

Definition: The rectifier which conducts current (voltage) during both positive and negative half-cycles of the ac input is called Full Wave rectifier.

@ Centre tapped full wave rectifier:

Circuit diagram and input & output Waveforms:

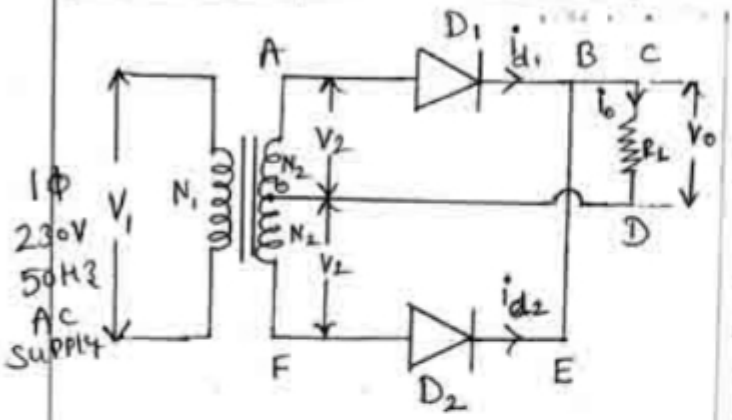
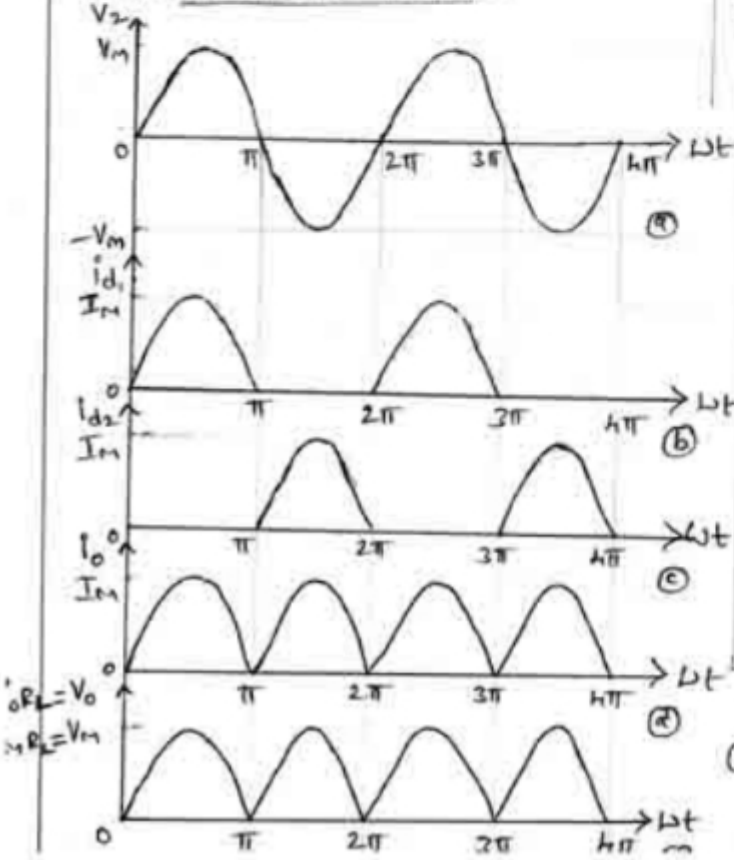


Fig: Full wave rectifier



Construction:

It consists of step down transformer with a centre-tapped secondary winding, two diodes and a load resistor. The input signal is applied to the primary winding of the transformer. The centre-tapped secondary winding of the transformer is connected to two diodes.

Operation:

→ During positive half cycle of the input voltage, end A becomes positive w.r.t end F. Hence the diode D_1 conducts & D_2 is off & the current flows through R_L (path: ABCDOA) (i_{d1})

(a) Secondary voltage Waveform
(b) & (c) Diode current Waveforms
(d) Load current Waveform

→ During negative half cycle of the input voltage, end f becomes negative w.r.t end F. Hence the diode D_2 conducts & D_1 is off & the current flows through R_L (Path: FEBCDOF) (i_{d2})

Therefore, the current flows through R_L in the same direction (C to D) for both half-cycles of input ac voltage.

Note:

① Advantages & Merits of Centre-tapped FWR:

(i) The dc output voltage and load current are twice than those of a HWR.

(ii) The ripple factor is much less (0.482) than that of a HWR (1.21)

(iii) The efficiency (81.2%) is twice that of HWR (40.6%)

(iv) The T.U.F (Transformer utilization factor) is more

(v) No D.C Saturation of transformer secondary winding takes place.

② Disadvantages & Drawbacks & Demerits of Centre-tapped FWR:

(i) The output voltage is half of the secondary voltage

(ii) The peak-inverse voltage (PIV) of a diode is twice that of the diode used in the HWR.

(iii) It is difficult to locate the centre tap on the secondary winding.

(iv) Higher PIV diodes are larger in size & Costlier.

(v) It is expensive to manufacture a Centre-tapped transformer, which produces equal voltages on each half of the secondary winding.

③ Current through diode (or) Current through R_L (I_o)

& Peak load current (I_m):

Instantaneous supply voltage is,

$$V_1 = V_m \sin \omega t \quad -(28)$$

Instantaneous secondary voltage is,

$$V_2 = \frac{N_2}{N_1} V_1 \quad -(29)$$

Using (28) in (29), we get

$$V_2 = V_m \sin \omega t \quad -(30) \quad (\text{Let } N_1 = N_2)$$

The equivalent circuit when the diode D_1 is ON & D_2 is OFF is shown below,

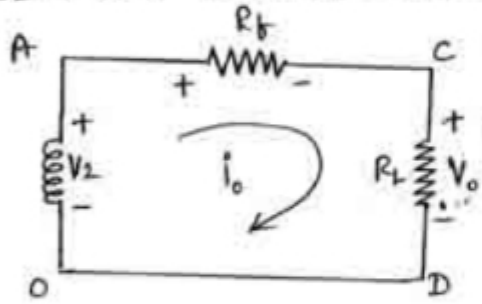


Fig: Equivalent circuit during positive half cycle of ac voltage

Applying KVL to the loop,

$$V_2 - i_o R_f - I_o R_L = 0$$

$$\Rightarrow i_o = \frac{V_2}{R_f + R_L}, \quad 0 \le \omega t \le \pi \quad -(31)$$

Using (30) in (31), we get

$$i_o = \frac{V_m}{R_f + R_L} \sin \omega t, \quad 0 \le \omega t \le \pi$$

$$\Rightarrow \boxed{i_o = I_m \sin \omega t \; ; 0 \le \omega t \le \pi} \quad -(32)$$

Where, $\boxed{I_m = \frac{V_m}{R_f + R_L}} \quad -(33)$

$R_f \rightarrow$ Forward resistance of the diode.

Eqn (32) gives the current through R_L

Eqn (33) gives the peak load current.

Derivations:

① Average load current (or) DC load current (or) DC output current (or) Average output current (I_{dc}):

DC load current,

$$I_{dc} = \frac{\text{Area under one cycle of } i_o}{\text{Period of } i_o}$$

$$= \frac{\int_0^{\pi} i_o \, d\omega t}{\pi}$$

$$= \frac{1}{\pi}\left[\int_0^{\pi} I_m \sin\omega t \, d\omega t\right] \quad \text{(Using 32)}$$

$$= \frac{I_m}{\pi}\left[-\cos\omega t\right]_0^{\pi}$$

$$\boxed{I_{dc} = \frac{2I_m}{\pi} \text{ or } 0.636\, I_m} \quad -(34) \quad (\because \cos\pi = -1, \cos 0 = 1)$$

(2) Average load voltage or DC load voltage or DC output voltage or Average output voltage (V_{dc}):

DC load voltage,

$$V_{dc} = I_{dc} R_L$$

$$= \frac{2I_m}{\pi} R_L \quad \text{(Using 34)}$$

$$= \frac{2}{\pi}\left[\frac{V_m}{R_f + R_L}\right] R_L \quad \text{(Using 33)}$$

$$\boxed{V_{dc} = \frac{2V_m/\pi}{1 + R_f/R_L}} \quad -(35)$$

If diode is ideal, $R_f = 0$

$$\therefore \boxed{V_{dc} = \frac{2V_m}{\pi} \text{ or } 0.636\, V_m} \quad -(36)$$

Note: ① Comparing (9) & (32), we can write, $I_{dc\,FWR} = 2\, I_{dc\,HWR}$

② Ripple Factor From (10) or (11) & (35) or (36)

(3) V_{dc} = Area under one cycle of V_o / Period of V_o

$$= \frac{\int_0^{\pi} V_o \, d\omega t}{\pi}$$

$$= \frac{\int_0^{\pi} i_o R_L \, d\omega t}{\pi} \quad [\because V_o = i_o R_L]$$

$$= \frac{1}{\pi}\left(\int_0^{\pi} i_o \, d\omega t\right) R_L$$

$$\Rightarrow = \frac{2V_m/\pi}{1 + R_f/R_L} \quad \text{(Same as (35))}$$

③ RMS load current (I_{rms}):

RMS load current.

$$I_{rms} = \sqrt{\frac{\text{Area under one cycle of } i_o^2}{\text{Period of } i_o}}$$

$$= \sqrt{\frac{\int_0^{\pi} i_o^2 \, d\omega t}{\pi}}$$

$$= \sqrt{\frac{1}{\pi}\left[\int_0^{\pi} I_m^2 \sin^2 \omega t \, d\omega t\right]} \quad \text{(Using 32)}$$

$$= \sqrt{\frac{I_m^2}{\pi}\int_0^{\pi}\left(\frac{1-\cos 2\omega t}{2}\right) d\omega t} \quad \left(\because \sin^2\theta = \frac{1-\cos 2\theta}{2}\right)$$

$$= I_m \sqrt{\frac{1}{2\pi}\left\{(\omega t)_0^{\pi} - \left(\frac{\sin 2\omega t}{2}\right)_0^{\pi}\right\}} \quad (\because \sin 2\pi = \sin 0 = 0)$$

$$= I_m \sqrt{\frac{1}{2\pi}(\pi)}$$

$$\boxed{I_{rms} = \frac{I_m}{\sqrt{2}}} \quad -(37)$$

Note: ① Comparing (12) & (37), we can write $I_{rms}(FWR) = \sqrt{2}\, I_{rms}(HWR)$ or $1.414\, I_{rms}(HW)$

② Similarly from (13) or (14) & (38) or (39), we can write $V_{rms}(FWR) = \sqrt{2}\, V_{rms}(HWR)$ or $1.414\, V_{rms}(HWR)$

④ RMS load voltage (V_{rms}):

RMS load voltage.

$$V_{rms} = I_{rms} R_L$$

$$= \frac{I_m}{\sqrt{2}} R_L \quad \text{(Using 37)}$$

$$= \frac{1}{\sqrt{2}} \frac{V_m}{R_f + R_L} R_L \quad \text{(Using 33)}$$

$$\boxed{V_{rms} = \frac{V_m/\sqrt{2}}{1 + R_f/R_L}} \quad -(38)$$

If diode is ideal, $R_f = 0$

$$\therefore \boxed{V_{rms} = \frac{V_m}{2}} \quad -(39)$$

(09)

$$V_{rms} = \sqrt{\frac{\text{Area under one cycle of } V_o^2}{\text{Period of } V_o}}$$

$$= \sqrt{\frac{\int_0^{\pi} V_o^2 \, d\omega t}{\pi}}$$

$$= \sqrt{\frac{1}{\pi}\int_0^{\pi} i_o^2 R_L^2 \, d\omega t} \quad (\because V_o = i_o R_L)$$

$$= \sqrt{\frac{1}{\pi}\int_0^{\pi} i_o^2 \, d\omega t} \times R_L$$

$$= \frac{I_m}{\sqrt{2}} R_L$$

$$\Rightarrow = \frac{V_m/\sqrt{2}}{\ldots} \quad \text{(Same as (38))}$$

(5) **Ripple factor (γ):**

Ripple factor,

$$\gamma = \frac{V_{ac}}{V_{dc}} \quad \text{---(*)}$$

$$= \frac{\sqrt{V_{rms}^2 - V_{dc}^2}}{V_{dc}} \quad \text{(using 18)}$$

$$= \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{V_m/\sqrt{2}}{1 + R_f/R_L}\right)^2 \Big/ \left(\frac{2V_m/\pi}{1 + R_f/R_L}\right)^2 - 1} \quad \text{(using 35 \& 38)}$$

$$= \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1}$$

$$\boxed{\gamma = 0.483 \text{ (or) } 48.3\% \quad \text{-(40)}}$$

(or)

$$\gamma = \frac{I_{ac}}{I_{dc}}$$

$$= \sqrt{\frac{I_{rms}^2 - I_{dc}^2}{I_{dc}}} \quad \text{(using 1)}$$

$$= \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1}$$

$$= 0.483 \text{ (Same as (40))}$$

From (*) & (40), we can write

$$\gamma = \frac{V_{ac}}{V_{dc}} = 48.3\%.$$

$$\Rightarrow V_{ac} = 48.3\% \text{ of } V_{dc}$$

(6) **Efficiency (or) Rectification efficiency (or) Power conversion efficiency (η)**

Efficiency,

$$\eta = \frac{P_{dc}}{P_{ac}} \quad \text{---(**)}$$

$$= \frac{I_{dc}^2 R_L}{I_{rms}^2 (R_f + R_L)}$$

$$= \frac{(2I_m/\pi)^2 R_L}{(I_m/\sqrt{2})^2 (R_f + R_L)}$$

$$= \frac{8}{\pi^2} \frac{R_L}{R_f + R_L}$$

$$\boxed{\eta = 81.2\% \text{ (or) } 0.812 \quad \text{-(41)}}$$

If diode is ideal, $R_f = 0$

$$\boxed{\eta = 0.812 \text{ (or) } 81.2\% \quad \text{-(42)}}$$

Note: ① From (**) & (42), we can write

$$\eta = \frac{P_{dc}}{P_{ac}} = 81.2\% \Rightarrow \boxed{P_{dc} = 81.2\% \text{ of } P_{ac}} \quad -(43)$$

② From (22) & (42), we can write

$$\eta(FWR) = 2\,\eta(HWR)$$

---

⑦ Percentage regulation or Voltage regulation (% Regulation)

$$\% \text{ Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 \quad -(44)$$

$$= \frac{\frac{2V_m}{\pi} - \frac{(2V_m/\pi)R_L}{R_f + R_L}}{\frac{(2V_m/\pi)R_L}{R_f + R_L}} \times 100$$

$$= \frac{\frac{2V_m}{\pi}\left(1 - \frac{R_L}{R_f + R_L}\right)}{\frac{2V_m}{\pi}\left(\frac{R_L}{R_f + R_L}\right)} \times 100$$

$$= \frac{\frac{R_f + R_L - R_L}{R_f + R_L}}{\frac{R_L}{R_f + R_L}} \times 100$$

$$\boxed{\% \text{ Regulation} = \frac{R_f}{R_L} \times 100} \quad -(45)$$

If diode is ideal, $R_f = 0$

$$\therefore \boxed{\% \text{ Regulation} = 0} \quad -(46)$$

$$V_{FL} = V_{dc} = \frac{2V_m/\pi}{1 + R_f/R_L}$$

$$\Rightarrow V_{FL} = \frac{(2V_m/\pi)R_L}{R_f + R_L}$$

&

$$V_{NL} = V_{dc}\big|_{R_L = \infty} = \frac{(2V_m/\pi)}{1 + R_f/\infty}$$

$$V_{NL} = \frac{2V_m}{\pi} \quad \left(\because \frac{R_f}{\infty} = 0\right)$$

From (25) & (45),

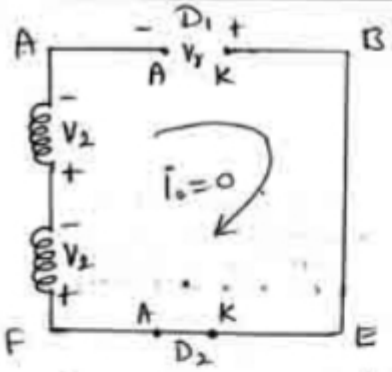
% Regulation for HWR = % Regulation for FWR

---

⑧ Peak inverse Voltage or Peak reverse Voltage (PIV)

The equivalent circuit of FWR when D_1 is ON & D_2 is OFF is shown in fig (*)

(67) The equivalent circuit of FWR when D_1 is OFF & D_2 is ON is shown in fig (**)



Fig(**): During negative half cycle of input

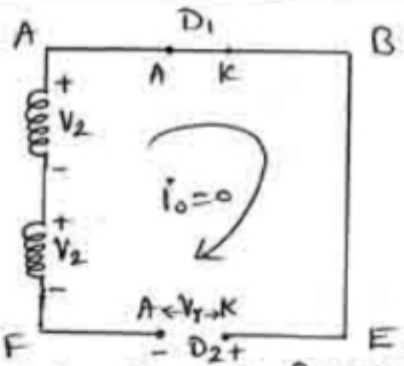
Applying KVL to the loop.

$-V_2 - V_2 + V_r = 0$

$\Rightarrow \quad V_r = 2V_2$

$\Rightarrow \quad V_r = 2V_m \sin\omega t$

$\Rightarrow \quad \boxed{PIV = V_{rmax} = 2V_m}$ (Using 30) —(47)



Fig(*): During positive half cycle of input

Applying KVL to the loop.

$+V_2 + V_2 - V_r = 0$

$\Rightarrow \quad V_r = 2V_2$

$\Rightarrow \quad V_r = 2V_m \sin\omega t$

$\Rightarrow \quad \boxed{PIV = V_{rmax} = 2V_m}$ (Using 30) —(47)

Note: From (27) & (47), we can write

$(PIV)_{FWR} = 2(PIV)_{HWR}$

(b) Full-wave bridge rectifier:

Circuit diagram:

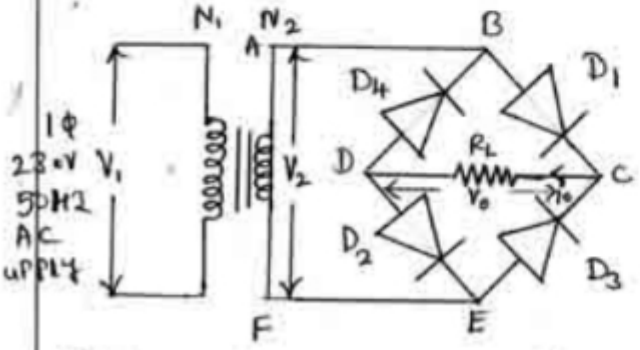


Fig: Full-wave bridge rectifier

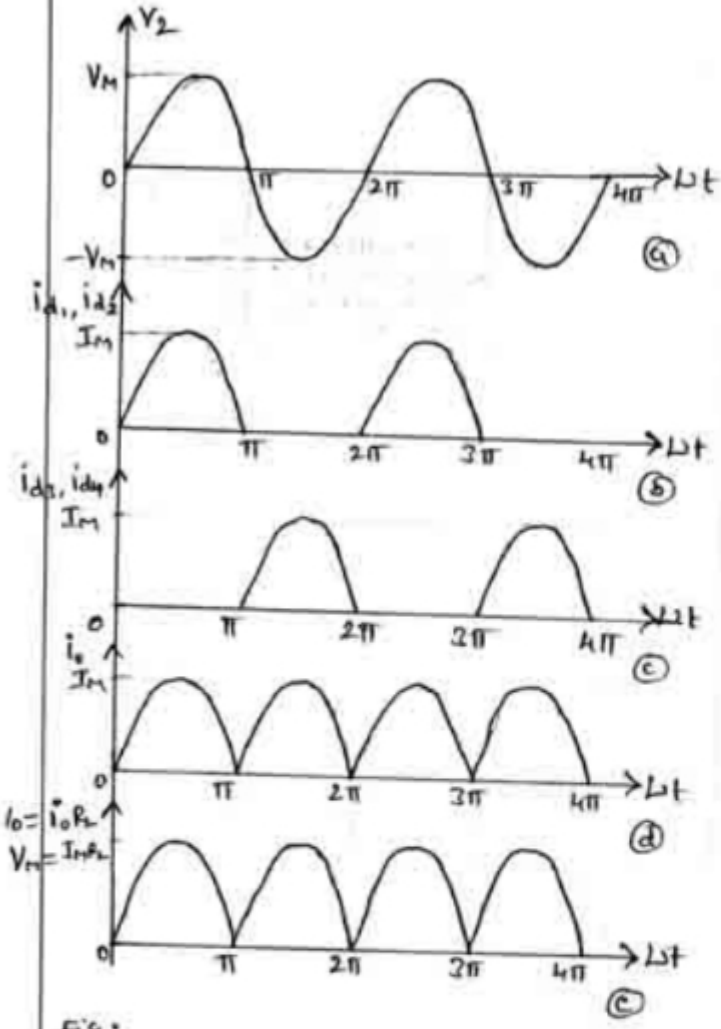
Construction:

It consists of a step down transformer, four diodes & a load resistor. The primary coil of a transformer is connected to ac input and secondary coil to a load resistor (R_L) through diodes.

Operation:

→ During positive half cycle of the input voltage, end A [illegible] positive w.r.t end C. Hence the diodes D_1 & D_3 are

ON & D_3 and D_4 are OFF. The current flows through R_L (Path: A B C D E F A)



→ During negative half cycle of the input voltage, end A becomes negative w.r.t end F. Hence the diodes D_3 & D_4 are ON & D_1 & D_2 are OFF. The current flows through R_L (Path: F E C D B A F)

Therefore, the current flows through R_L in the same direction (C to D) for both half-cycles of input ac voltage.

Fig:
(a) Secondary voltage Wave form (b) & (c) Diodes current Waveforms
(d) Load current Wave form (e) Load Voltage Wave form.

Note:

(i) Advantages (ii) Merits of Full-Wave bridge rectifier

(i) The center-tapped transformer is not required.
(ii) The transformer is less costly.
(iii) The PIV is one-half that of the Centre-tap circuit.
(iv) The output is twice that of the Centre-tap circuit for the same secondary voltage.

(v) The T.U.F (Transformer utilization factor) is more.
(vi) Less D.C Saturation of transformer Secondary winding
(vii) It can be used in applications where floating output terminals are allowed.

② Disadvantages (or) Draw backs (or) Demerits of Full wave bridge rectifier:

(i) It requires four diodes
(ii) As during each half-cycle of a.c input two diodes that conduct are in series, therefore, voltage drop in the internal resistance of the rectifying unit will be twice as compared to centre tap circuit.

③ Current through R_L (i_o) & peak load current (I_m):

Instantaneous supply voltage is,

$$V_1 = V_m \sin \omega t \quad -(48)$$

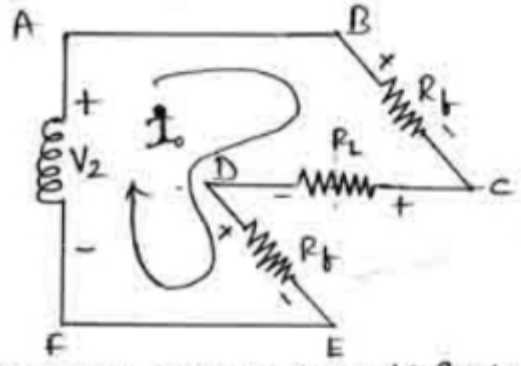
Instantaneous secondary voltage is.

$$V_2 = \frac{N_2}{N_1} V_1 \quad -(49)$$

Using (48) in (49), & assuming $N_1 = N_2$, we can write.

$$V_2 = V_m \sin \omega t \quad -(50)$$

The equivalent circuit when the diodes D_1 & D_2 are ON & the diodes D_3 & D_4 are off is shown below.



Equivalent circuit during +ve cycle

Applying KVL to the loop

$$V_2 - i_o R_f - i_o R_L - i_o R_f = 0$$

$$\Rightarrow i_o = \frac{V_2}{2R_f + R_L}, \quad 0 \le \omega t \le \pi \quad -(51)$$

Using (50) in (51), we get

$$i_o = \frac{V_m}{2R_f + R_L} \sin \omega t, \quad 0 \le \omega t \le \pi$$

$$\Rightarrow \boxed{i_o = I_m \sin\omega t \; ; \; 0 \le \omega t \le \pi} \quad -(52)$$

Where, $\boxed{I_m = \frac{V_M}{2R_f + R_L}} \quad -(53)$

Where, $R_f \rightarrow$ Forward resistance of the diode

Eqn (52) gives the current through R_L

Eqn (53) gives the peak load current @ maximum load current

Derivations

(1) Average load current @ DC load current @ DC output current @ Average output current (I_{dc}):

$$I_{dc} = \frac{\text{Area under one cycle of } i_o}{\text{Period of } i_o}$$

$$\boxed{I_{dc} = \frac{2I_m}{\pi} \approx 0.636 I_m \approx \frac{2V_m/\pi}{2R_f + R_L}} \quad (\text{Using } 53) \quad -(54)$$

(2) Average load voltage @ DC load voltage @ DC output voltage @ Average output voltage (V_{dc}):

$$V_{dc} = I_{dc} R_L$$

$$= \frac{2I_m}{\pi} R_L \quad (\text{Using } 54)$$

$$\boxed{V_{dc} = \frac{2V_m/\pi}{1 + 2(R_f/R_L)}} \quad -(55) \quad (\text{Using } 53)$$

If diode is ideal, $R_f = 0$

$$\therefore \boxed{V_{dc} = \frac{2V_m}{\pi} \approx 0.636 V_m} \quad -(56)$$

(3) RMS load current (I_{rms}):

$$I_{rms} = \sqrt{\frac{\text{Area under one cycle of } i_o^2}{\text{Period of } i_o}}$$

$$\boxed{I_{rms} = \frac{I_m}{\sqrt{2}} \approx \frac{V_m/\sqrt{2}}{2R_L + 0}} \quad -(57) \quad (\text{Using } 53)$$

4) RMS load voltage (V_{rms}):

$V_{rms} = I_{rms} R_L$

$$V_{rms} = \frac{V_m/\sqrt{2}}{1 + 2(R_f/R_L)} \quad -(58)$$

If diode is ideal, $R_f = 0$.

$$\therefore V_{rms} = \frac{V_m}{\sqrt{2}} \quad -(59)$$

5) Ripple factor (γ):

$$\gamma = \frac{V_{ac}}{V_{dc}}$$

$\gamma = 0.483$ @ 48.3% —(60)

6) Efficiency @ Rectification efficiency @ Power conversion efficiency (η):

$$\eta = \frac{P_{dc}}{P_{ac}}$$

$$\eta = \frac{0.812}{1 + 2(R_f/R_L)} \quad -(61)$$

If diode is ideal, $R_f = 0$

$\therefore \eta = 0.812$ @ 81.2% —(62)

7) Percentage regulation @ Voltage regulation (% Regulation):

$$\% \text{ Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

$$= \frac{\frac{2V_m}{\pi} - \frac{(2V_m/\pi) R_L}{2R_f + R_L}}{\frac{(2V_m/\pi) R_L}{2R_f + R_L}} \times 100$$

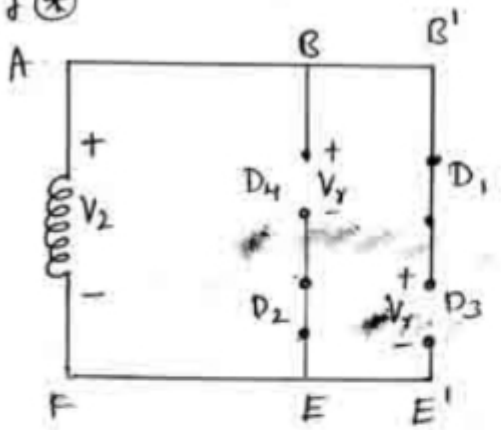
$$\% \text{ Regulation} = \frac{2R_f}{R_L} \times 100 \quad -(63)$$

If diode is ideal, $R_f = 0$

$\therefore$ % Regulation = 0 —(64)

8) Peak inverse voltage @ Peak reverse voltage (PIV) @ (PRV)

The equivalent circuit of full wave bridge rectifier when D_1 & D_2 are ON and D_3 & D_4 are OFF is shown in fig (*)



Applying KVL to ABEFA

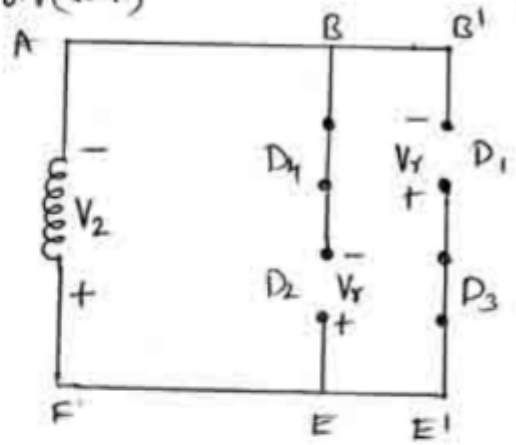
$V_2 - V_r = 0$ (ABB'E'EFA)

$\Rightarrow V_r = V_2 = V_m \sin \omega t$ (Using (i))

$\Rightarrow$ **PIV = $V_{rmax} = V_m$**

Note: (i) $f_{out} = 2 f_{in}$
(FWR o/p freq) = (2 × i/p freq)

(ii) The equivalent circuit of full wave bridge rectifier when D_3 & D_4 are ON and D_1 & D_2 are OFF is shown in fig (**)



Applying KVL to AEFA
(ii) ABB'E'EFA

$-V_2 + V_r = 0$

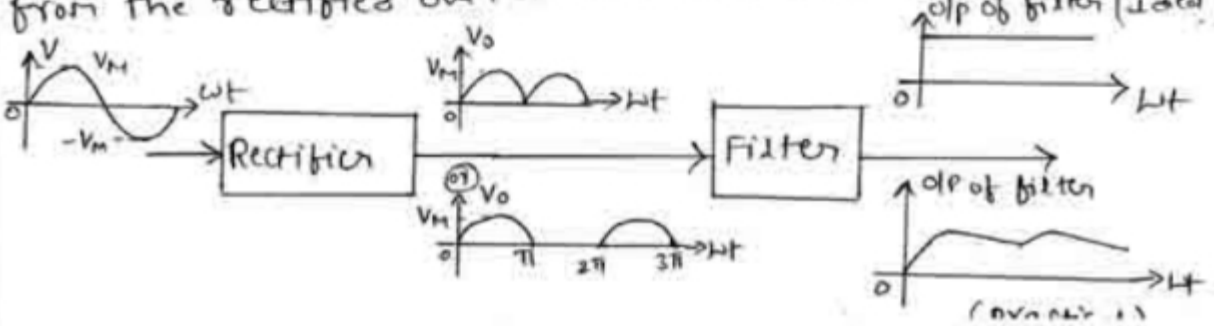
$\Rightarrow V_r = V_2 = V_m \sin \omega t$

$\Rightarrow$ **PIV = $V_{rmax} = V_m$**

* Filters (ii) Filter circuits:

The output of the rectifier is pulsating dc ie it contains ac and dc components.

A device which (filters out) removes the a.c component (ripples) from the rectified output is called filter.



The most commonly used filter circuits are ① Capacitor filter ② Inductor filter ③ Choke input (LC) filter ④ π - filter (Capacitor input)

① HWR with Capacitor filter:

Fig ① shows a HWR with capacitor filter.

Fig ② shows different waveforms

- The reactance of a capacitor is $X_C = \frac{1}{2\pi f C}$
- For dc, $f = 0$. $\therefore X_C = \infty$ i.e capacitor offers infinite reactance to d.c (Capacitor passes ac signal but blocks dc)

→ During the positive half-cycle of the ac input voltage, the diode is forward biased (conducts) and it charges the capacitor to the peak value of secondary transformer voltage (V_m) (indicated by oa). The charging time is negligible.

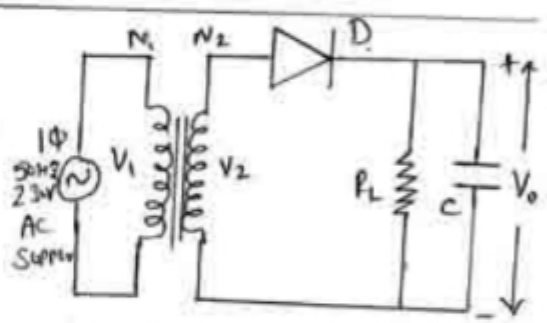
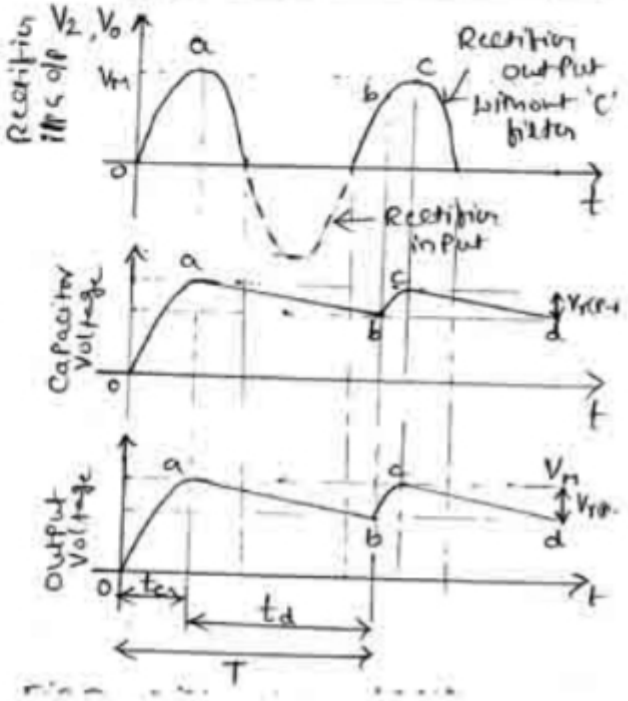


Fig ①: HWR with capacitor filter

When the ac input voltage falls below V_m, the capacitor discharges through the load resistance (indicated by ab). This discharging of the capacitor continues until the diode starts conducting again. This process is repeated again and again. and the output voltage waveform becomes 'oabcd'



The ripple factor with 'C' filter is,

$$\gamma = \frac{1}{2\sqrt{3} f R_L C}$$

$f \rightarrow$ Frequency of the supply Hz
$R_L \rightarrow$ Load resistance
$C \rightarrow$ Capacitance value of capacitor

Note: ① The process of removing ac components (ripples) from the rectified output is called filtering.

② The discharging time (t_d) is,

$$t_d = C \cdot R_L$$

where, $C \rightarrow$ capacitance value of the capacitor
$R_L \rightarrow$ Load resistance.

③ Without capacitor filter, output varies between Zero & V_M
With capacitor filter, output varies between $[V_M - V_{r(P-P)}]$ & V_M

④ $V_{r(P-P)} = \frac{I_{dc}}{fC} = \frac{V_{dc}}{fCR_L}$

$V_{r(P-P)} \rightarrow$ Peak to Peak ripple voltage on capacitor.

⑤ $V_{dc} = V_M - \frac{I_{dc}}{2fC} = V_M - \frac{V_{dc}}{2fCR_L}$

⑥ $V_{dc} = \frac{V_M}{\left(1 + \frac{1}{2fCR_L}\right)}$

② Full Wave rectifier with Capacitor filter:

Fig ③ shows a FWR with capacitor filter.

Fig ④ shows different waveforms.

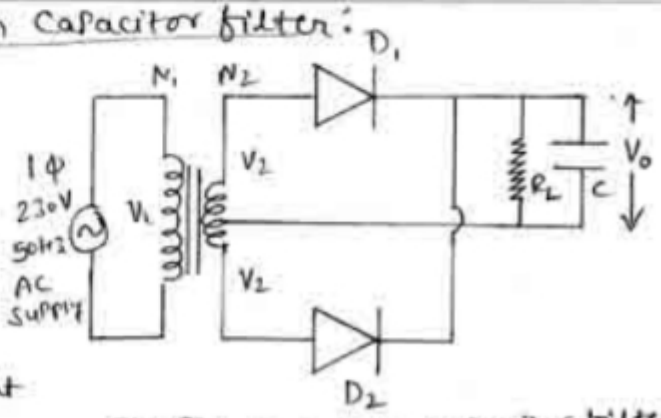


Fig ③: FWR with capacitor filter

→ During the positive half-cycle of the ac input voltage, the diode D_1 is forward biased and it charges the capacitor to the peak value of secondary transform

Voltage (V_M) (indicated by oa). When the transformer Secondary Voltage falls below V_M, the capacitor discharges through the load resistance (D, Stops Conducting) and this continues until the diode D_2 start conducting again (ab). This process is repeated again and again and the output waveform becomes oabcdefg

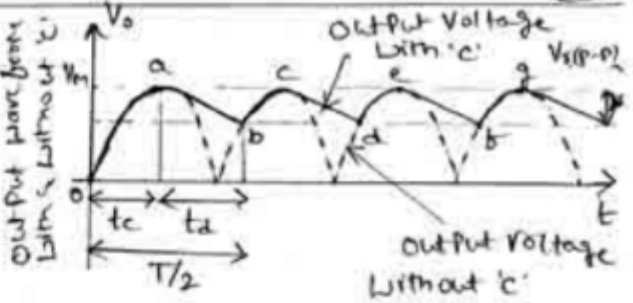


Fig 4: Different Waveforms

The ripple factor with 'c' filter is,

$$\gamma = \frac{1}{4\sqrt{3} f R_L C}$$

③ Full Wave bridge rectifier with Capacitor filter:

Fig ⑤ shows a FW bridge rectifier with capacitor filter.

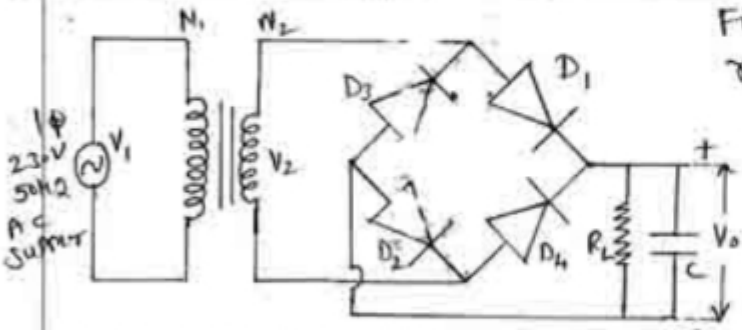


Fig 5: Full Wave bridge rectifier with Capacitor filter

Fig ⑥ Shows different Waveforms.

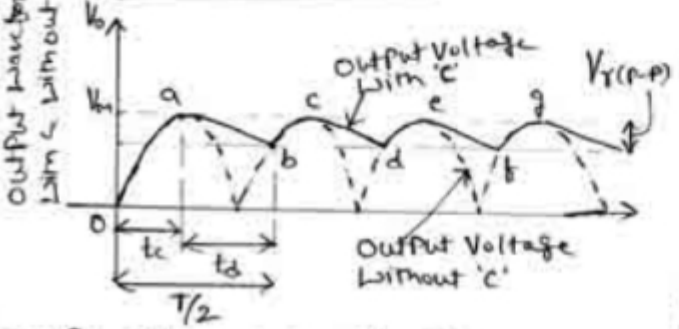


Fig ⑥: Different Waveforms

→ During the positive half-cycle of the ac input voltage, diodes D_1 and D_2 conduct & charge the capacitor to the peak value of the secondary transformer voltage (V_M) (indicated by oa). When the transformer Secondary Voltage falls below V_M (D_1 & D_2 stop Conducting), the capacitor discharges through the load resistance and this continues

until the diodes D_3 & D_4 start conducting (indicated by ab again. This process is repeated again & again and output waveform becomes 'oabcdefg'

The ripple factor with 'C' filter is,

$$\gamma = \frac{1}{4\sqrt{3} f R_L C}$$

Note: ① $V_{r(P-P)} = \frac{I_{dc}}{2fc} = \frac{V_{dc}}{2fcR_L}$

② $V_{dc} = V_M - \frac{I_{dc}}{4fc} = V_M - \frac{V_{dc}}{4fcR_L}$ (or)

$$V_{dc} = \frac{V_M}{1 + \frac{1}{4fcR_L}}$$

} For FW center tap rectifier & FW bridge rectifier

③ Advantages of capacitor filter:

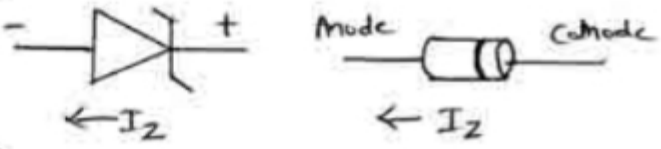
(i) Low cost (ii) Small size (iii) Little weight
(iv) Good characteristics (v) An inexpensive filter for light loads (ie load with larger value of resistance)
~~(vi) Good value of~~
(vi) Suitable for small load currents (say upto 50mA)
[used in transistor radio battery eliminators]

④ Disadvantages of capacitor filter:

(i) Not suitable for heavy loads (ie a load with smaller values of resistance)
(ii) Ripple factor depends on load resistance

Note: ① Zener diode

(i) Circuit Symbol:



(ii) Junction breakdown:

When a junction diode is reverse biased, a very small

reverse saturation current flows through the diode. Zener diodes are the diodes which are designed to operate in the breakdown region. They are also called as breakdown & Avalanche diodes

When the reverse voltage is sufficiently increased, the junction breaks down and a large reverse current flows. If a resistor (R_1) is connected in series with the diode, the current is limited & will not destroy the device.

(iii) Voltage regulators:

A circuit which converts unregulated dc to regulated (constant) dc is called voltage regulator

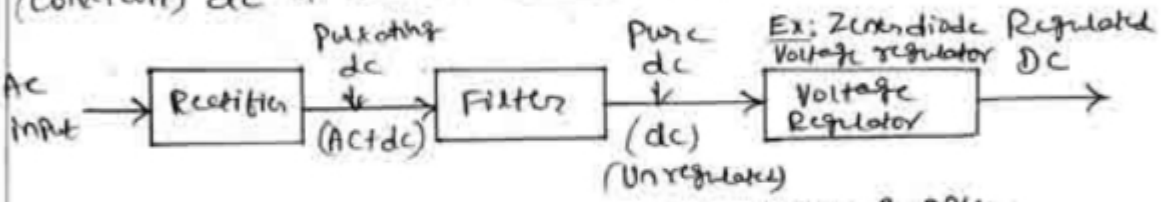


Fig: Block diagram of Regulated dc power supply

Zener diode Voltage regulators:

Under reverse bias condition, the voltage across the Zener diode remains constant (even input changes). Hence Zener diode is sometimes called as voltage regulator

The Zener current (I_Z) must satisfy the condition

$$I_{ZK} < I_Z < I_{ZM}$$

I_Z should be selected as I_{ZT} (Specified test current (usually 20mA))

Where I_{ZK} → Diode Knee voltage & minimum reverse current to sustain breakdown

I_{ZM} → maximum Zener current limited by the maximum power dissipation (P_D)

$$P_D = V_Z I_{ZM}$$

① Zener diode Voltage regulator Under no load (or) (Regulator circuit with no load) (or) Under no load

Fig shows the Zener Voltage regulator with no load

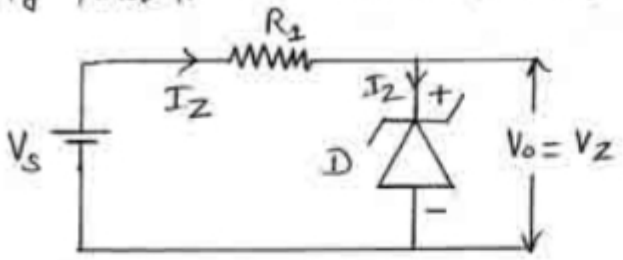


Fig: Zener voltage regulator with no load

→ V_S is the unregulated dc voltage (output from rectifier with filter) greater than the Zener breakdown voltage (V_Z).

→ Here o/p $V_o = V_Z$ → Constant

→ Current I_Z must satisfy the condition.

$$I_{ZK} < I_Z < I_{ZM}$$

Where
I_{ZK} → minimum Zener current to sustain breakdown
I_{ZM} → maximum Zener current (to have power dissipation less than the maximum permissible value (PD))

→ Normally I_Z is selected as I_{ZT} (specified test current).

→ Applying KVL to the loop

$$V_S - I_Z R_1 - V_Z = 0$$

$$\Rightarrow I_Z = \frac{V_S - V_Z}{R_1} \quad \text{(or)} \quad R_1 = \frac{V_S - V_Z}{I_Z}$$

Minimum Zener current,

$$I_{Z\min} = \frac{V_{S\min} - V_Z}{R_1}$$

Maximum Zener current,

$$I_{Z\max} = \frac{V_{S\max} - V_Z}{R_1}$$

→ Power dissipated in R_1,

$$P_{R_1} = I_Z^2 R_1$$

② Loaded regulator (or) Loaded Zener voltage regulator (or) (Shunt regulator)

Fig shows the zener voltage regulator with load

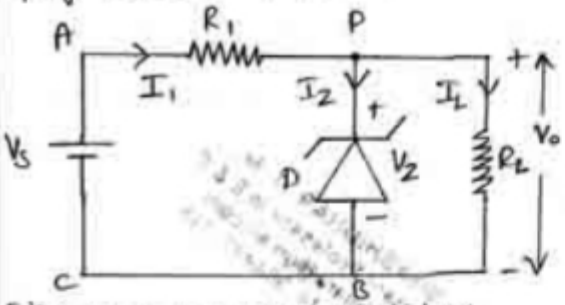


Fig: Zener Voltage regulator with load

→ V_s is the unregulated dc voltage (output from rectifier with filter)

→ Voltage across R_L = Voltage across zener diode

i.e $V_o = V_z$ — ①

→ We have from KCL at node P.

$$I_1 = I_z + I_L \quad — ②$$

→ Applying KVL to loop APBC, we get.

$$V_s - I_1 R_1 - V_z = 0$$

$$\Rightarrow \quad I_1 = \frac{V_s - V_z}{R_1} \quad — ③$$

→ When $I_L = I_{L\max}$, $I_z = I_{z\min}$, we get (From eqn 2)

$$I_1 = I_{z\min} + I_{L\max} \quad — ④$$

For a zener diode with $I_{ZT} = 20mA$, $I_{z\min} = 5mA$

→ When $I_L = 0$, entire I_1 flows through the zener diode.

We should ensure that the total current doesnot exceed the maximum zener diode current (I_{zm}). Now eqn ② becomes,

$$I_1 = I_{zm} \quad — ⑤ \qquad [\because I_z = I_{zm},\ I_L = 0 \text{ in eqn ②}]$$

→ Equating ④ & ⑤, we get

$$I_{zm} = I_{z\min} + I_{L\max} \quad — ⑥$$

→ Using ⑤ in ③, we get

$$I_{zm} = \frac{V_s - V_z}{R_1} \quad — ⑦ \qquad R_1 = \frac{V_s - V_z}{I_{zm}} \quad — ⑧$$

Note: ① If input voltage V_s varies

Using ② & ③, $I_Z = \left(\frac{V_s - V_Z}{R_1}\right) - I_L$

$\Rightarrow \frac{V_{s\min} - V_Z}{R_1} - I_{L\max} > I_{Z\min}$ ④ $R_{1(\max)} = \frac{V_{s\min} - V_Z}{I_{Z\min} + I_{L\max}}$

& $\frac{V_{s\max} - V_Z}{R_1} - I_{L\min} < I_{Z\max}$ ⑤ $R_{1(\min)} = \frac{V_{s\max} - V_Z}{I_{Z\max} + I_{L\min}}$

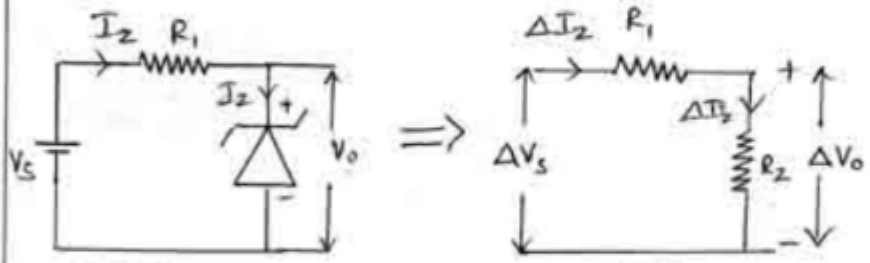
② Power Supply Performance

The dc output voltage in a dc power supply varies due to

ⓐ Source effect ⓑ Load effect

① Source effect

Without load



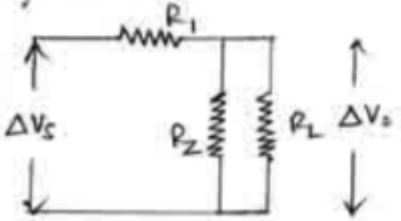
Fig① Fig②

→The Equivalent circuit of zener voltage regulator under no load is shown in fig②.

→From voltage divider rule,

$$\Delta V_o = \frac{\Delta V_s \, R_Z}{R_1 + R_Z}$$

With load



(or)

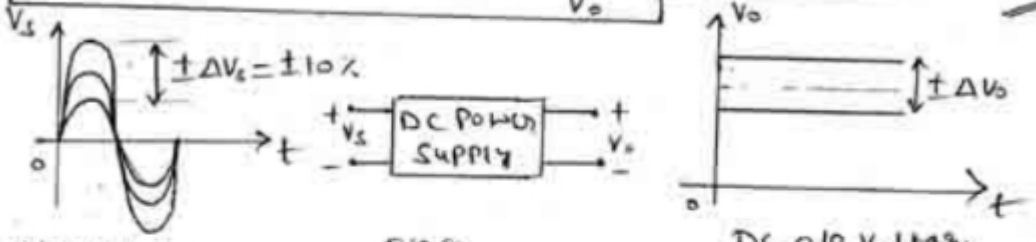
$$\Delta V_o = \frac{\Delta V_s (R_Z \| R_L)}{R_1 + (R_Z \| R_L)}$$

→The change in the output voltage (ΔV_o) due to the change in the line voltage (ac supply voltage) is called Source effect

ie Source effect = ΔV_o for a 10% change in V_s

→ The Source effect expressed as a percentage of the dc output voltage V_o is called the line regulation (or) Source regulation

ie line regulation = $\frac{\Delta V_o \text{ for a } 10\% \text{ change in } V_s}{V_o} \times 100\ \%$



AC i/p Voltage

Fig ③

DC o/p Voltage

(b) Load effect:

Thevenin's equivalent circuit of the Zener voltage regulator with load is shown in fig ④

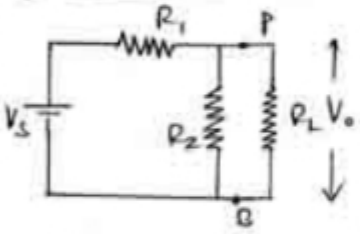


Fig ④

$$\Delta V_{Th} = \Delta I_L (R_1 \| R_2)$$

→ The change in load voltage is due to the change in voltage ΔV_{Th}, which is due to change in current.

→ The change in the output voltage (ΔV_o) due to the change in the load current (ΔI_L) is called load effect.

ie load effect = ΔV_o for ΔI_L

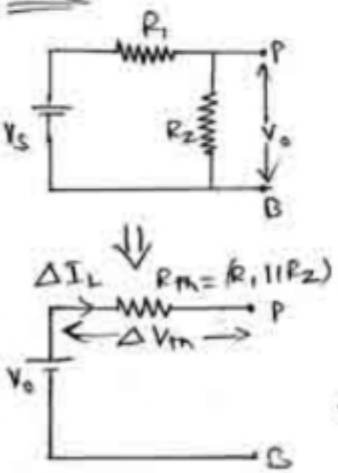


Fig ⑤

→ The load effect expressed as a percentage of the dc output voltage (V_o) is called the load regulation

ie load regulation = $\frac{\Delta V_o \text{ for } \Delta I_L}{V_o} \times 100\ \%$

Problems:

① Determine the levels of reverse saturation current at temperature of 35°c and 45°c for a junction which has $I_o = 30nA$ at 25°c.

Sol: Given $I_o(T_1) = 30 \times 10^{-9} A$ at $T_1 = 25°c$

$I_o(T_2) = ?$ at $T_2 = 35°c$

W.K.T

$$I_o(T_2) = I_o(T_1)\left[2^{(T_2 - T_1)/10}\right]$$

$$I_o(T_2) = 30 \times 10^{-9}\left[2^{(35-25)/10}\right]$$

$$\boxed{I_o(T_2) = 60nA} \text{ at } T_2 = 35°c$$

$I_o(T_2) = ?$ at $T_2 = 45°c$

$$I_o(T_2) = 30 \times 10^{-9}\left[2^{(45-25)/10}\right]$$

$$\boxed{I_o(T_2) = 120nA} \text{ at } T_2 = 45°c$$

② A Silicon pn-junction has a reverse saturation current of $I_o = 30nA$ at a temperature of 300k. Calculate the junction current when the applied voltage is (a) 0.7V forward bias, (b) 10V reverse bias.

Sol:

(a) Given $I_o = 30 \times 10^{-9} A$.

$T = 300k$.

$V_D = 0.7V$

W.K.T

$$I_D = I_o\left(e^{V_D/\eta V_T} - 1\right)$$

$$= 30 \times 10^{-9}\left(e^{13.46} - 1\right)$$

$$\boxed{I_D = 21mA}$$

$$\left(\because \frac{V_D}{\eta V_T} = \frac{V_D}{\eta \cdot KT/q} = \frac{0.7}{2 \times 1.38 \times 10^{-23} \times 300 / 1.6 \times 10^{-19}} = 13.46\right)$$

(b) Given $I_o = 30 \times 10^{-9} A$

$T = 300k$

$V_D = -10V$

$$I_D = 30 \times 10^{-9}\left(e^{-192} - 1\right)$$

$$\boxed{I_D = -30nA}$$

$$\left(\frac{V_D}{\eta V_T} = \frac{-10}{2 \times 1.38 \times 10^{-23} \times 300 / 1.6 \times 10^{-19}} = -192\right)$$

③ A Silicon Pn-junction has a reverse saturation current of 30nA at a temperature of 300k. Calculate the junction forward-bias voltage required to produce a current of (a) 0.1mA, (b) 10mA.

Sol: We have, $I_D = I_0(e^{V_D/\eta V_T} - 1)$

$\Rightarrow V_D = \eta V_T \ln\left(\frac{I_D}{I_0} + 1\right)$

Given, $\eta = 2$ (Si)

$I_0 = 30 \times 10^{-9}$ A

$T = 300$ K.

(a) $V_D = ?$ at $I_D = 0.1 \times 10^{-3}$ A

(b) $V_D = ?$ at $I_D = 10 \times 10^{-3}$ A

$V_T = 26 \times 10^{-3}$ V at $T = 300$K

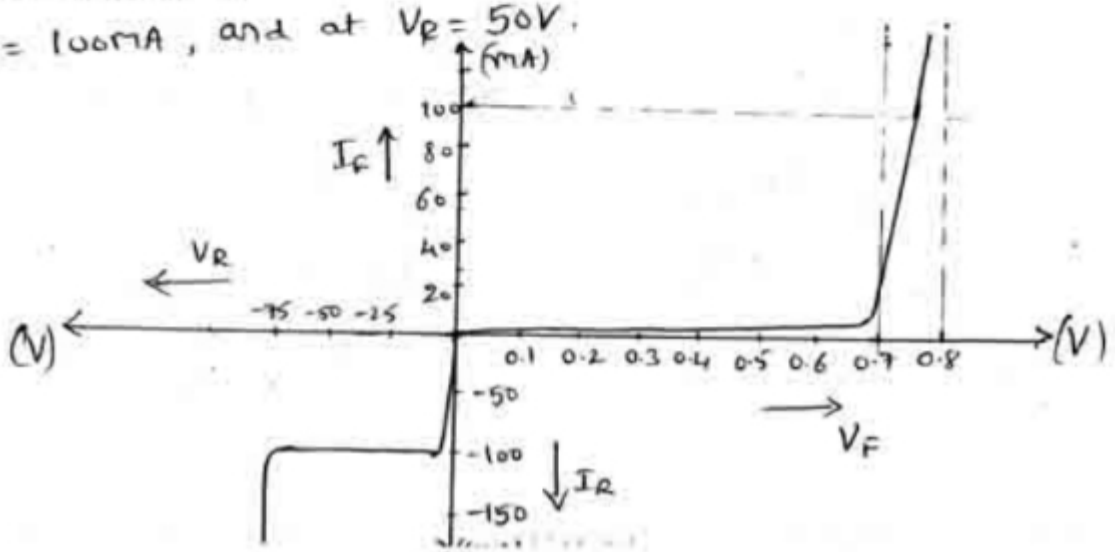
(a) $V_D = 2 \times 26 \times 10^{-3} \ln\left(\frac{0.1 \times 10^{-3}}{30 \times 10^{-9}} + 1\right)$

$\boxed{V_D = 421.8\text{mV}}$

(b) $V_D = 2 \times 26 \times 10^{-3} \ln\left(\frac{10 \times 10^{-3}}{30 \times 10^{-9}} + 1\right)$

$\boxed{V_D = 661.27\text{mV}}$ //

④ Calculate the forward and reverse resistances offered by a Silicon diode with the characteristics in fig ⊕ at $I_F = 100$mA, and at $V_R = 50$V.



Sol: From the characteristics,

At $I_F = 100mA$, $V_F \simeq 0.75V$

∴ Forward resistance,

$$R_F = \frac{V_F}{I_F}$$

$$= \frac{0.75}{100 \times 10^{-3}}$$

$$\boxed{R_F = 7.5\Omega}$$

At $V_R = 50V$, $I_R \simeq 100nA$

∴ Reverse resistance,

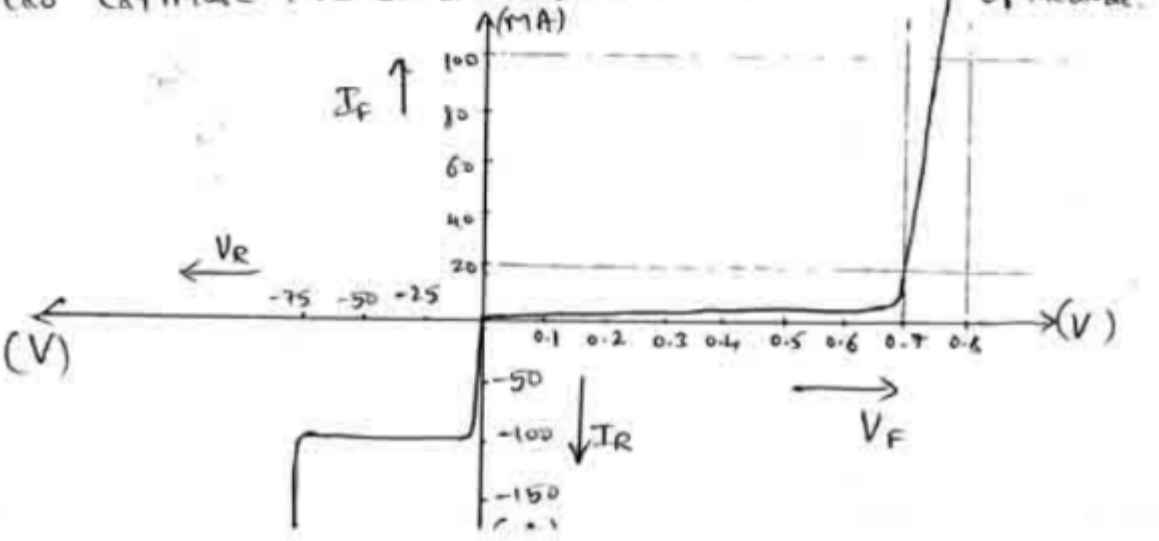
$$R_R = \frac{V_R}{I_R}$$

$$= \frac{50}{100 \times 10^{-9}}$$

$$\boxed{R_R = 500M\Omega}$$

∴ $I_R << I_F$ &
$R_R >> R_F$

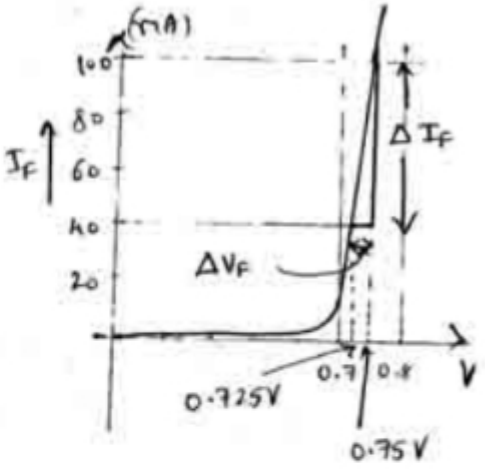
⑤ Determine the dynamic resistance at a forward current of 70mA for the diode characteristics given in fig ⑤. Also estimate the diode dynamic resistance & cut-in voltage of the diode.



Sol:
Dynamic resistance, is,

$$r_d = \frac{\Delta V_F}{\Delta I_F} = \frac{V_{F_2} - V_{F_1}}{I_{F_2} - I_{F_1}}$$

Let us take two points on the curve at (70mA ± 30mA)



At $I_{F_2} = 100mA$, $V_{F_2} =$

At $I_{F_1} = 40mA$, $V_{F_1} =$

$$\therefore r_d = \frac{0.75 - 0.725}{100\times10^{-3} - 40\times10^{-3}}$$

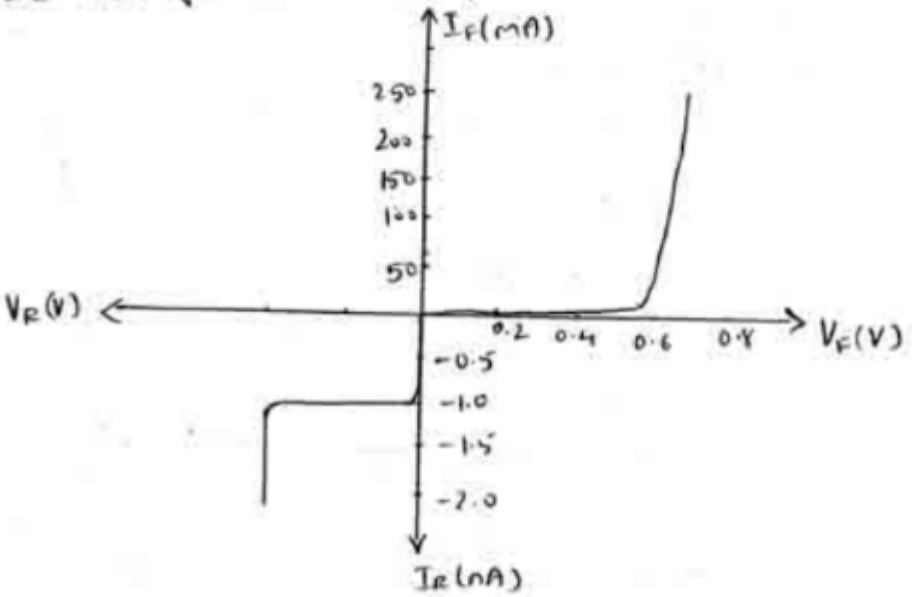
$$\boxed{r_d = 0.4166\ \Omega}$$

Diode dynamic resistance

$$r_d' = \frac{26\times10^{-3}V}{I_F} = \frac{26\times10^{-3}}{70\times10^{-3}} = 0.371\ \Omega$$

From the knee of the characteristics, $V_K = 0.7V$

(6) From the characteristics shown below identify the diode and give its ratings.



Sol: From the knee of the characteristics.

$$V_\gamma \simeq 0.6V$$

∴ Diode used in the given characteristics is a Silicon diod

Ratings:

Maximum forward current, $I_{F(max)} = 250mA$

Cut-in voltage, $V_\gamma = 0.6V$

Reverse saturation current, $I_0 = 1nA$

Reverse breakdown voltage $V_{BR} = 100V$

Maximum reverse voltage, $V_{R(max)} = 75V$ (75% of 100V)

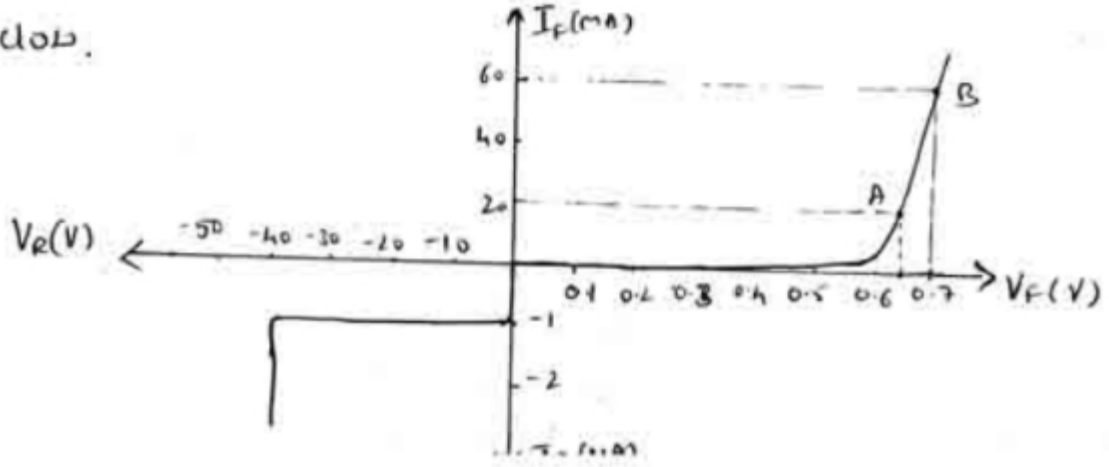
⑦ Plot the forward & reverse characteristics of a diode, given the following data:

Cut-in voltage = 0.6V, Reverse breakdown voltage = 40V, Nominal reverse current = 1μA, Forward current = 20mA at a forward voltage of 0.65V. Forward current = 60mA at a forward voltage of 0.7V.

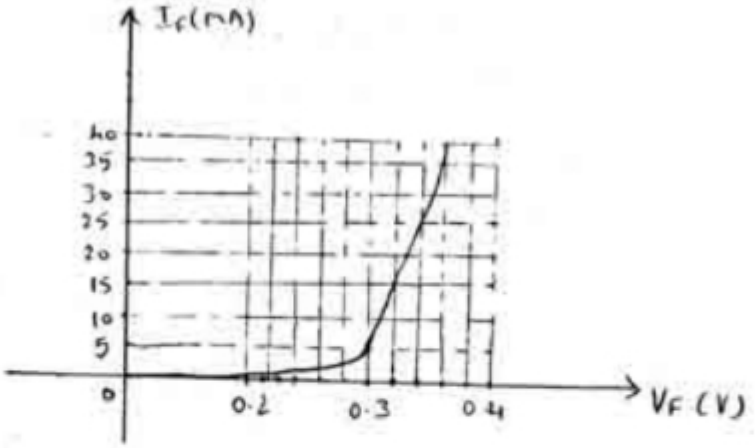
Sol: Given, $V_\gamma = 0.6V$, $I_0 = 1\mu A$, $V_{BR} = 40V$,

$I_F = 20mA$ at $V_F = 0.65V$ (Point A). $I_F = 60mA$ at $V_F = 0.7V$ (Point B)

The forward & reverse characteristics of the diode is shown below.



(8) Find the static forward resistance at a forward current of 20mA for the diode whose characteristics is shown below. Further, find the dynamic resistance at 20mA using (i) the characteristics and (ii) the forward current. Estimate the value of the substrate resistance.



Sol:

Static forward resistance,

$$R_F = \frac{V_F}{I_F} = \frac{0.33V}{20\times10^{-3}A} = 16.5\Omega$$ (At $I_F = 20mA$, $V_F = 0.33V$)

(i) Dynamic resistance from the characteristics,

$$r_d = \frac{\Delta V_F}{\Delta I_F} = \frac{V_{F2} - V_{F1}}{I_{F2} - I_{F1}} = \frac{0.35 - 0.31}{(30-10)\times10^{-3}} = 2\Omega$$

(ii) Dynamic resistance using forward current (Pure ac resistance)

$$r_d' = \frac{0.026}{I_F} = \frac{0.026}{20\times10^{-3}} = 1.3\Omega$$

Substrate resistance,

$$r_{substrate} = r_d - r_d' = 2 - 1.3 = 0.7\Omega$$

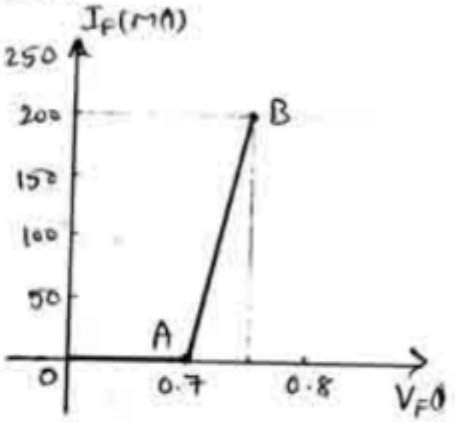
At $I_{F_1} = 20mA - 10mA = 10mA$ $V_{F_1} = 0.31V$

At $I_{F_2} = 20mA + 10mA = 30mA$ $V_{F_2} = 0.35V$

⑨ Construct the piecewise linear characteristic for a Si diode that has a 0.25Ω dynamic resistance and a 200mA maximum forward current.

Sol:

Cut in voltage of Si diode, $V_\gamma = 0.7V$



Step 1: Draw the voltage and current axis.

Step 2: Mark Point A at $V_F = 0.7V$ on the V_F axis ie A(0.7, 0)

Step 3: By definition,

$$r_d = \frac{\Delta V_F}{\Delta I_F}$$

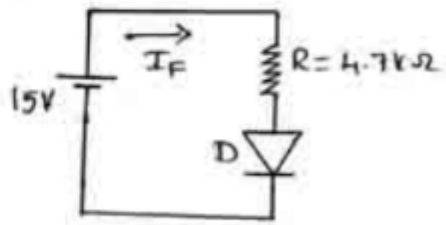
$$\Rightarrow \Delta V_F = r_d \times \Delta I_F = 0.25 \times 200 \times 10^{-2} = 0.05\,V$$

$$\therefore V_F = 0.7 + 0.05 = 0.75\,V$$

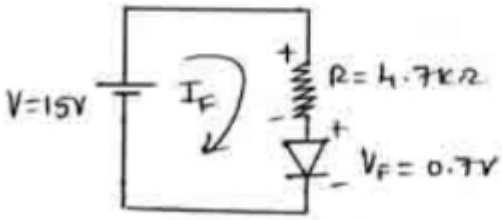
Now mark Point B at $V_F = 0.75V$ & $I_F = 200mA$ ie B(0.75, 200 $\times 10^{-3}$)

Step 4: Join AB to get the piecewise linear characteristic of Si diode

⑩ A Silicon diode is used in the circuit shown in fig ⑲. Calculate the diode current.



Sol:

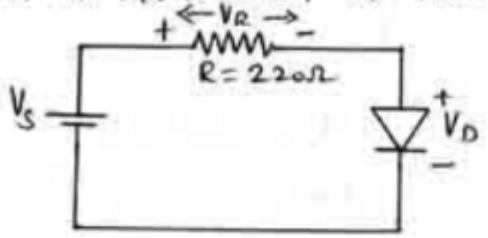


Applying KVL to the loop,

$$V - I_F R - V_F = 0$$

$$\Rightarrow I_F = \frac{V - V_F}{R} = \frac{15 - 0.7}{4.7 \times 10^3} = 3.042\,mA$$

(11) A diode is in series with 220Ω and the voltage across the resistor is 4V. What is the current through the diode?



Sol: Current through the diode is,

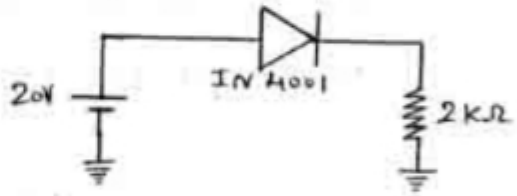
I_D = Current through resistor

= Voltage across the resistor / Resistance

= 4 / 220

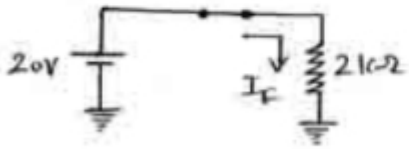
$I_D = 18.18mA$ //

(12) Calculate the load current for the circuit shown in fig (12). (Ideal diode)



Sol:

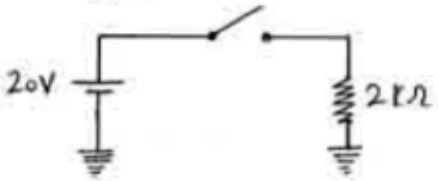
During Forward bias



$I_F = \frac{20V}{2 \times 10^3 \Omega}$

$I_F = 10mA$

During reverse bias



$I_F = 0$ //

(13) In fig (13), Calculate the load current, load voltage, load power, diode power and total power.

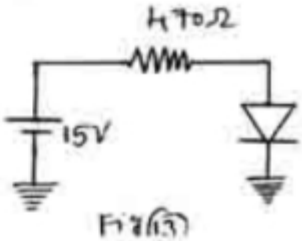


Fig (13)

Sol: Given $V = 15V$, $R = 470\Omega$

Load Current. $I_R = \frac{15}{470} = 3.2 \times 10^{-2} A$ //.

Load Voltage. $V_R = I_R \times R = 3.2 \times 10^{-2} \times 470 = 15V$

(∵ Diode is ideal)

Load Power $P_D = I_R \times V_R = 3.2 \times 10^{-2} \times 15 = 0.48W$ //.

Diode Power P_{diode} = Diode Vtg × Diode Current

$= 0$ //. (∵ Diode Voltage = 0,)

Total Power $P_t = V \times I = 15 \times 3.2 \times 10^{-2} = 0.48W$

(M) Calculate I_F for the diode circuit in fig (14). assuming that the diode has $V_F = 0.7V$ and $r_d = 0$. Then recalculate the current taking $r_d = 0.25\Omega$.

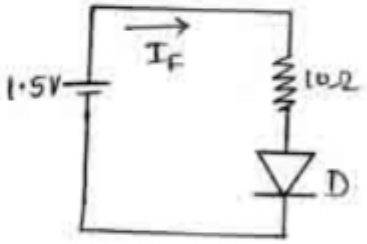
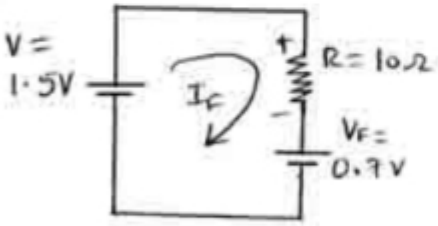


Fig (14)

Sol: With $r_d = 0$



Applying KVL

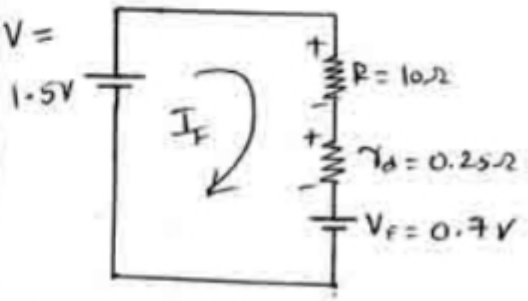
$+1.5 - I_F R - 0.7 = 0$

$\Rightarrow I_F R = 1.5 - 0.7$

$I_F = \frac{1.5 - 0.7}{10}$

$I_F = 80mA$ //.

With $r_d = 0.25\Omega$



Applying KVL

$1.5 - I_F R - I_F r_d - V_F = 0$

$\Rightarrow I_F = \frac{1.5 - 0.7}{10 + 0.25}$

$I_F = 78mA$ //.

(15) Find the value of resistor R in the circuit shown in fig (15). Given, dynamic resistance of the diode is 0.4Ω & the circuit current is 100mA.

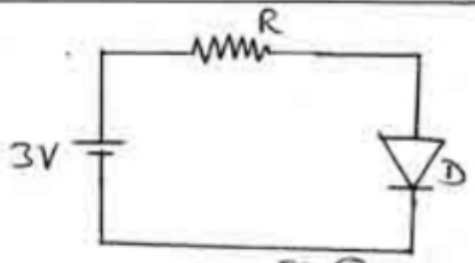
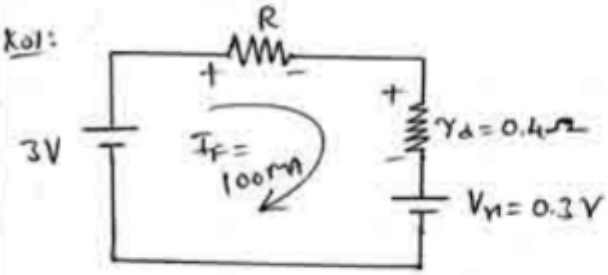


Fig (15)

Sol:



Applying KVL to loop

$$3 - RI_F - r_d I_F - V_\gamma = 0$$

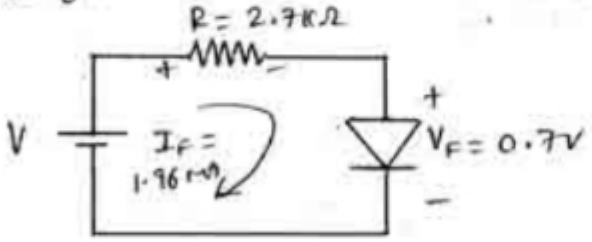
$$\Rightarrow R = \frac{3 - 0.4 \times 100 \times 10^{-3} - 0.3}{100 \times 10^{-3}}$$

$$= \frac{2.66}{100 \times 10^{-3}}$$

$$\boxed{R = 26.6\,\Omega}$$ //

(16) A circuit consists of a silicon diode in series with a 2.7kΩ resistor and a battery. Find the supply voltage if the forward current is 1.96mA.

Sol:



Applying KVL

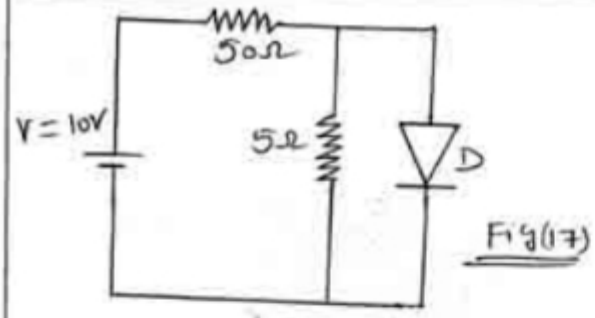
$$V - I_F R - V_F = 0$$

$$\Rightarrow V = I_F R + V_F$$

$$= 1.96 \times 10^{-3} \times 2.7 \times 10^{3} + 0.7$$

$$\boxed{V = 5.992\,V}$$

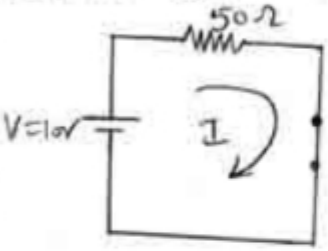
(17) Find the current through the diode in the circuit shown in fig (17). Assume diode to be ideal.



Fig(17)

Sol:

Since diode D is ideal, it acts as a short circuit. Resistor 5Ω can be neglected since it is in the line with SC.



∴ Current through the diode is,

$$I = \frac{V}{R} = \frac{10}{50} = 0.2A$$

(18) Determine the current I in the circuit shown in fig (18). Assume the diodes to be of Silicon and forward resistance of diodes to be zero.

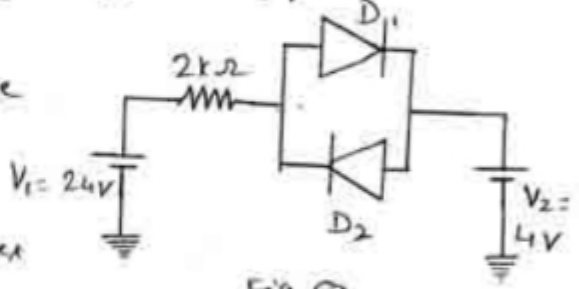
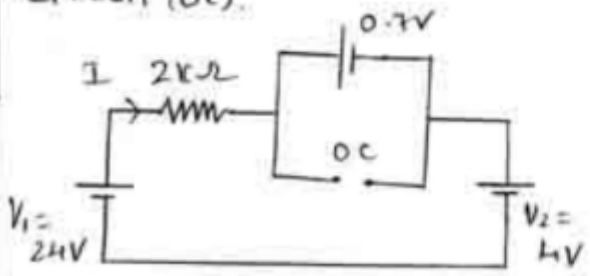


Fig (18)

Sol:

Here diode D_1 is forward biased and diode D_2 is reverse biased. ∴ D_1 acts as ~~short circuit (SC)~~ V/g source of 0.7V and D_2 acts as open circuit (OC).



Applying KVL,

$$V_1 - 2KI - 0.7 - V_2 = 0$$

$$\Rightarrow I = \frac{V_1 - V_2 - 0.7}{2 \times 10^3}$$

$$= \frac{24 - 0.7 - 4}{2 \times 10^3}$$

$$\boxed{I = 9.65mA}$$

(18) Find the voltage V_A in the circuit shown in fig (19).

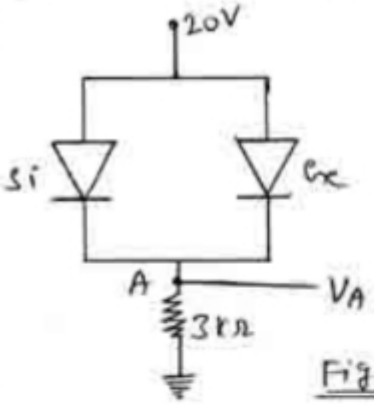


Fig (19)

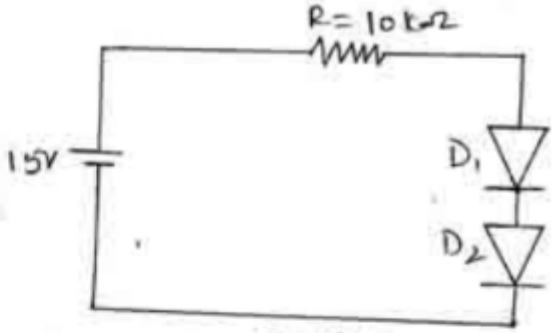
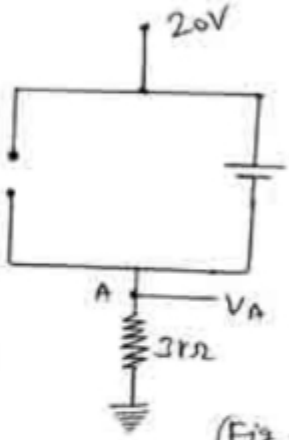


Fig (20)

Sol:

When voltage is applied, Ge diode ($V_\gamma = 0.3V$) will turn on first and a drop of 0.3V is maintained across the parallel circuit. The silicon diode never gets the opportunity to have 0.7V across it and therefore, remains in open-circuit state as shown in fig(*)

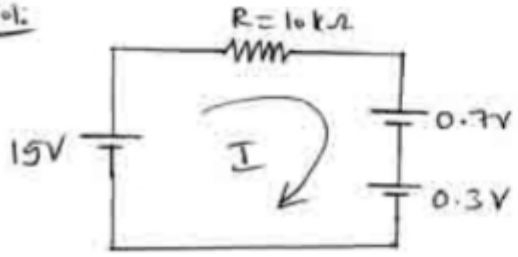


(Fig *)

$\therefore V_A = 20 - 0.3 = \underline{19.7V}$

(19) Calculate the diode current in the circuit shown in fig (20). Assume D_1 as Si diode and D_2 as Ge diode

Sol:



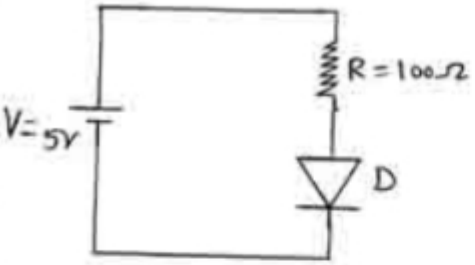
Applying KVL to the loop,

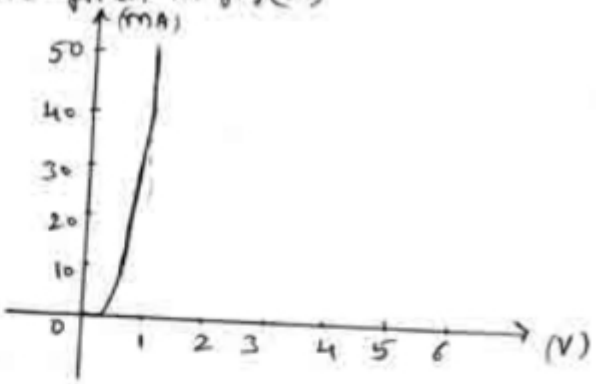
$15 - IR - 0.7 - 0.3 = 0$

$\Rightarrow I = \frac{15-1}{R} = \frac{14}{10 \times 10^3}$

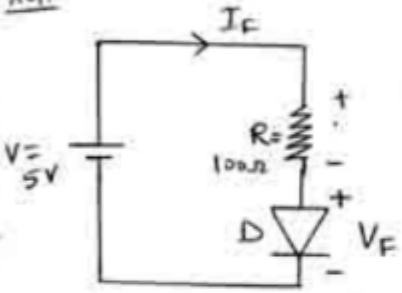
$\boxed{I = 1.4\,mA}$ //

(21) Draw the dc load line for the circuit in fig (21) on the diode forward characteristic given in fig(*)





Sol:



Applying KVL to the loop.

$$V - I_F R - V_F = 0$$

$$\Rightarrow \quad V = I_F R + V_F \quad -(*)$$

Put $I_F = 0$ in eqn (*)

$$V = V_F$$

$$\Rightarrow \boxed{V_F = V = 5V}$$

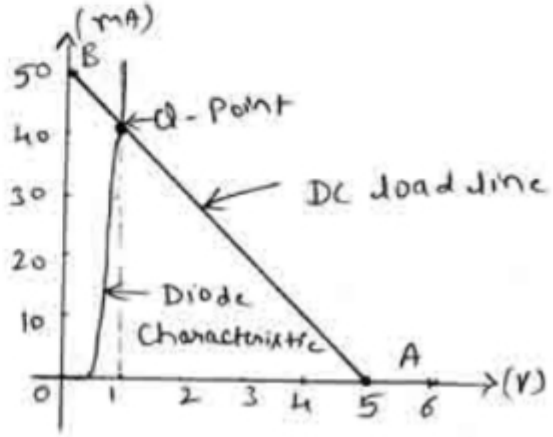
Put $V_F = 0$ in eqn (*)

$$V = I_F R$$

$$\Rightarrow \quad I_F = \frac{V}{R} = \frac{5}{100} = 50\,mA$$

Mark Point A at $V_F = 5V$ & $I_F = 0$ & Mark Point B at $V_F = 0$ & $I_F = 50\,mA$

Join AB to get the dc load line [fig(**)]



Fig(**)

(22) Using the device characteristics in fig (22), determine the required load resistance for the circuit in fig(***)

to give $I_F = 30mA$.

Read

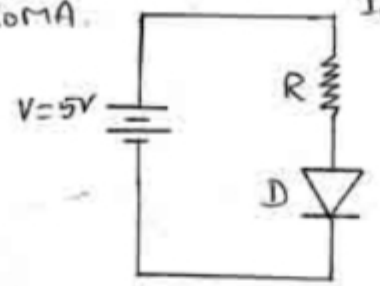


Fig (***)

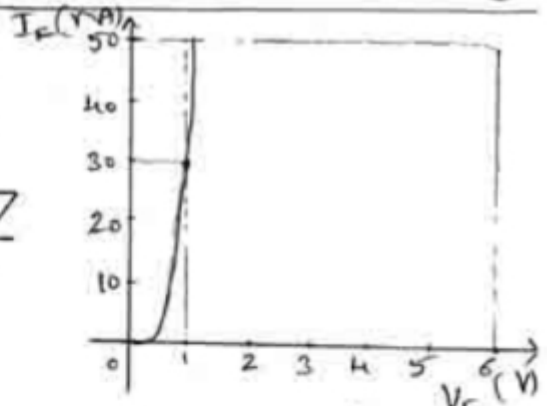
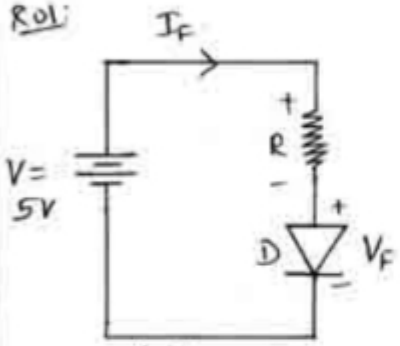


Fig (22)

Sol:



Applying KVL to the loop.

$$V - I_F R - V_F = 0$$

$$\Rightarrow V = I_F R + V_F$$

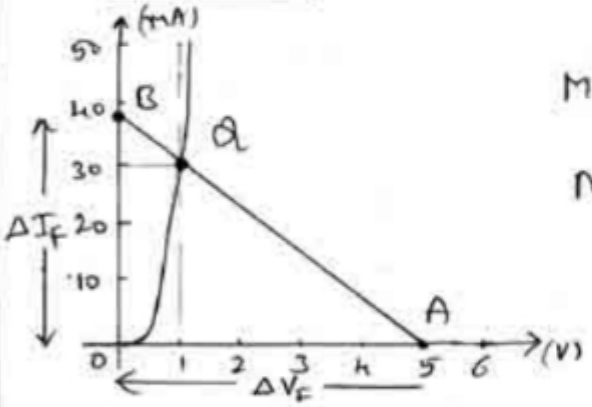
Put $I_F = 0$

$$\boxed{V_F = V = 5V}$$

Mark Point A at $V_F = 5V$ & $I_F = 0$

Now Plot Point Q at $I_F = 30mA$

Draw the dc load line from Point A through Q.



From the load line

$$R = \frac{\Delta V_F}{\Delta I_F} = \frac{5}{37.5 \times 10^{-3}} = 13\ \Omega$$

(23) Determine a new supply voltage for the circuit in fig (1) to give a 50mA diode forward current when $R = 100\Omega$. Also draw the dc load line on the characteristic given in fig (2)

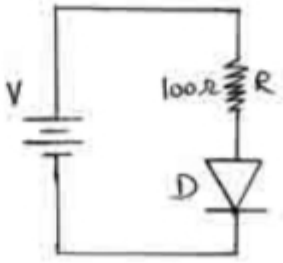


fig (1)

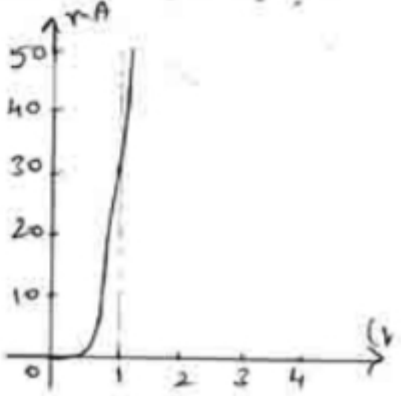


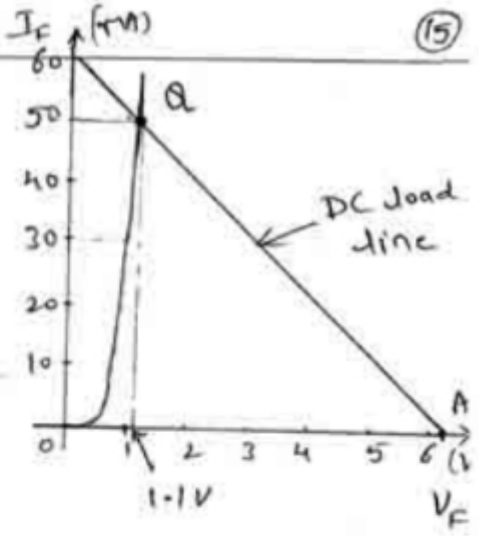
Fig (2)

Sol:

Plot Point Q on the diode Characteristic at $I_F = 50mA$

Project Point Q on V_F axis,

$\therefore V_F = 1.1V$



We know that

$$R = \frac{\Delta V_F}{\Delta I_F}$$

$$\Rightarrow \Delta V_F = \Delta I_F \times R = 50 \times 10^{-3} \times 100 = \underline{5V}$$

New Supply voltage,

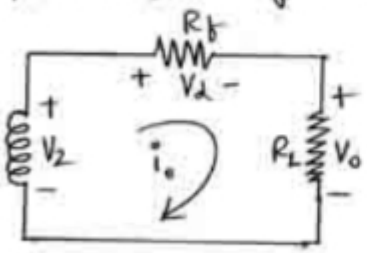
$$V = V_F + \Delta V_F = 1.1 + 5 = \underline{6.1V}$$

Mark Point A at $I_F = 0$ & $V_F = 6.1V$

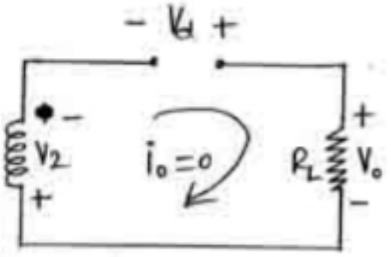
Draw dc load line through A & Q.

(b) S.T in a HWR, the dc voltage across the diode is equal but opposite in Polarity of the dc voltage across R_L.

Sol: The equivalent circuit when the diode is conducting & not conducting is shown below,



① Equivalent circuit when diode is conducting



② Equivalent circuit when diode is not conducting

Instantaneous diode Voltage (fig 1),

$$V_d = i_o R_f$$

$$\Rightarrow V_d = I_m R_f \sin \omega t, \quad 0 \leq \omega t \leq \pi \quad (\because i_o = I_m \sin \omega t)$$

Applying KVL to the loop of fig ②.

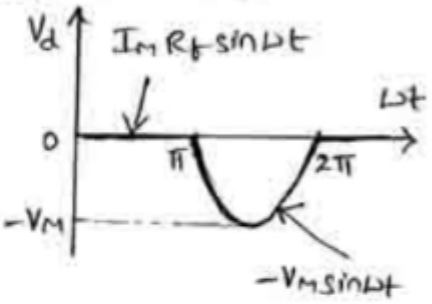
$-V_2 + V_d - i_o R_L = 0$, $\pi \le \omega t \le 2\pi$ $\quad (\because i_o = 0 \text{ \& } V_2 = V_m \sin \omega t)$

$\Rightarrow \quad V_d = V_2 = V_m \sin \omega t$, $\pi \le \omega t \le 2\pi$ $\quad -②$

From ① & ②, we can write

$$V_d = \begin{cases} I_m R_f \sin \omega t & ; \ 0 \le \omega t \le \pi \\ V_m \sin \omega t & ; \ \pi \le \omega t \le 2\pi \end{cases}$$

The voltage across diode 'V_d' is shown below (Assuming $R_f = 0$).



Average dc voltage across diode,

$$V_{dc}' = \frac{\text{Area under one cycle of } V_d}{\text{Period of } V_d}$$

$$= \frac{\int_0^{2\pi} V_d \, d\omega t}{2\pi}$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} 0 \, d\omega t + \int_{\pi}^{2\pi} V_m \sin \omega t \, d\omega t\right]$$

$$= \frac{1}{2\pi}\left[V_m (-\cos \omega t)_{\pi}^{2\pi}\right]$$

$$= \frac{V_m}{2\pi}(-\cos 2\pi + \cos \pi)$$

$$V_{dc}' = -\frac{V_m}{\pi} \quad (\because \cos \pi = -1, \ \cos 2\pi = 1)$$

$$\boxed{V_{dc}' = -V_{dc}} \quad -③ \quad \left(\because V_{dc} = \frac{V_m}{\pi}\right) \text{(from ⑪, Page ㉛)}$$

Eqn ③, shows that the dc voltage across the diode is equal but opposite in polarity of the dc voltage across R_L.

(25) Show that the power delivered to the load is maximum in a half-wave rectifier when the load resistance is equal to the forward resistance of the diode. Also find the maximum dc output power.

Sol: W.K.T $P_{dc} = \frac{V_{dc}^2}{R_L}$

$$\Rightarrow \quad P_{dc} = \frac{1}{R_L}\left[\frac{(V_m/\pi)\,R_L}{R_f + R_L}\right]^2 \qquad \left(\because V_{dc} = \frac{V_m/\pi}{1 + R_f/R_L}\right)$$

$$P_{dc} = \left(\frac{V_m}{\pi}\right)^2 \frac{R_L}{(R_f + R_L)^2} \quad \text{— (*)}$$

DC output power is maximum. When $\frac{dP_{dc}}{dR_L} = 0$

$$\Rightarrow \left(\frac{V_m}{\pi}\right)^2 \left\{\frac{(R_f+R_L)^2 \cdot 1 - R_L\, 2(R_f+R_L)}{(R_f+R_L)^4}\right\} = 0$$

$$\Rightarrow \quad (R_f + R_L)^2 - 2R_L(R_f + R_L) = 0$$

$$\Rightarrow \quad (R_f + R_L)(R_f + R_L - 2R_L) = 0$$

$$\Rightarrow \quad (R_f + R_L)(R_f - R_L) = 0$$

$$\Rightarrow \quad R_f - R_L = 0 \qquad (\because R_f + R_L \neq 0 \text{ or } R_f \neq -R_L)$$

$$\boxed{R_L = R_f}$$ // Hence Proof

Now maximum output dc power is,

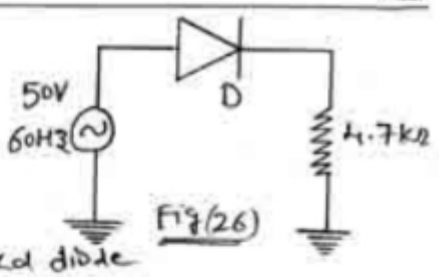
$$P_{d(max)} = \left(\frac{V_m}{\pi}\right)^2 \frac{R_L}{(R_f + R_L)^2}\Bigg|_{R_L = R_f}$$

$$= \left(\frac{V_m}{\pi}\right)^2 \frac{R_L}{(R_L + R_L)^2}$$

$$\boxed{P_{d(max)} = \left(\frac{V_m}{\pi}\right)^2 \frac{1}{4R_L} \text{ or } \left(\frac{V_m}{\pi}\right)^2 \frac{1}{4R_f}}$$

26 (a) What is the peak output voltage in the fig(26) if the diode is ideal? What is the average value? What is the dc value? Sketch the output waveform.

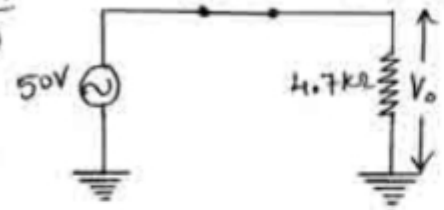
(b) Repeat part (a) if the ideal diode is replaced by a Si diode



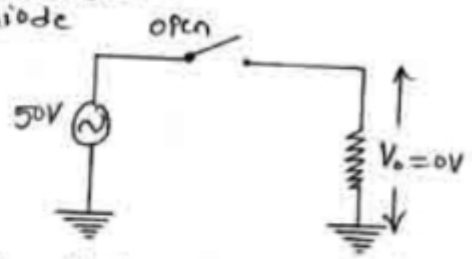
Fig(26)

Sol:

(a)



circuit in positive half cycle



circuit in negative half cycle

Given $V_{in} = 50V$ (rms)

$\therefore V_m = \sqrt{2}\, V_{in} = \sqrt{2} \times 50 = 70.710V$ → Peak output voltage (Peak input voltage)

D.K.T Average value & DC value

$$V_{dc} = \frac{V_m}{\pi} = \frac{70.710}{\pi} = 22.50V$$ → Average value & DC value

The diode conducts only for positive half cycle of input signal & the output waveform is shown in fig (*)

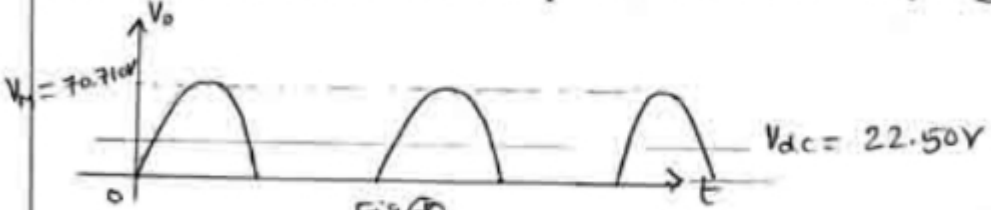
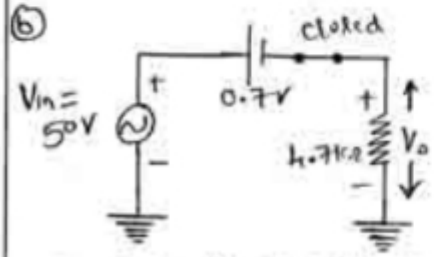
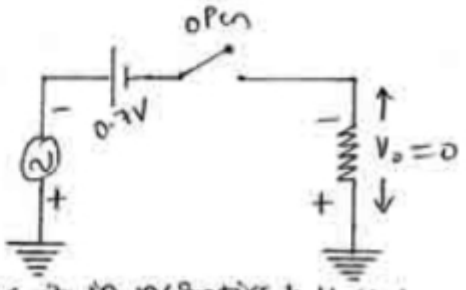


Fig (*)

(b)



circuit in positive half cycle



circuit in negative half cycle

Applying KVL to the loop

$V_{in} - 0.7 - V_o = 0$

$\Rightarrow \quad V_o = V_m - 0.7$

$$\Rightarrow (V_o)_M = (V_{in})_M - 0.7$$
$$= \sqrt{2} \times 50 - 0.7$$
$$= 70.010V \rightarrow \text{Peak output Voltage}$$

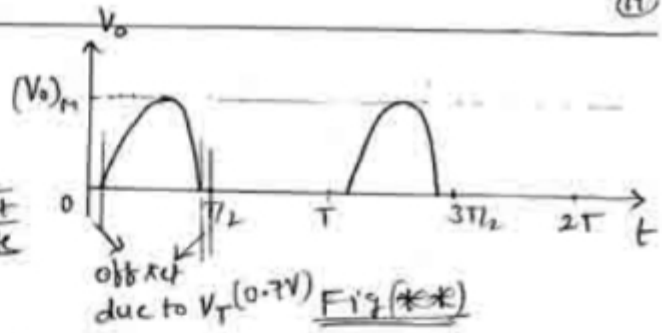


Fig (**)

Wkt Average @ DC Value is,

$$V_{dc} = \frac{(V_o)_M}{\pi} = \frac{70.010}{\pi} = 22.28V \rightarrow \text{Average Value @ DC Value}$$

The diode conducts only when the input voltage is atleast 0.7V. For levels of V_{in} less than 0.7V, the diode is still in an open-circuit state. The output waveform is shown in fig (**)

(27) (a) What is the peak output voltage in fig (27) if the diode is ideal? What is the average @ dc value? Sketch the output waveform

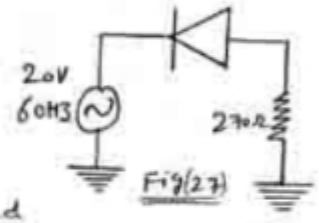
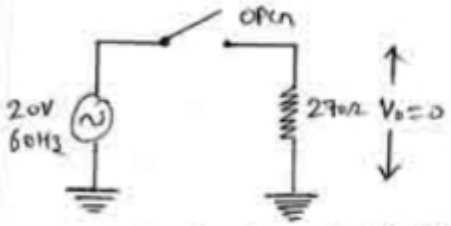


Fig (27)

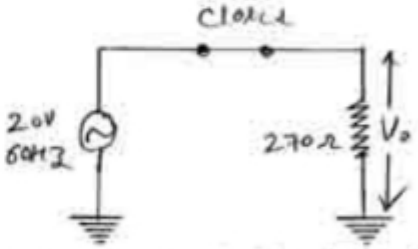
(b) Repeat Part (a) if the ideal diode is replaced by second approximation of the diode.

Sol:

(a) Let us assume the given diode as Si diode (Cut-in voltage = 0.7V)



Circuit in positive half cycle



Circuit in negative half cycle

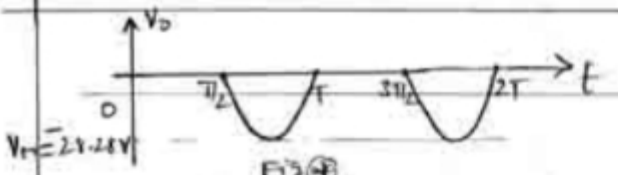
Given $V_{in} = 20V(rms)$

$\therefore V_m = \sqrt{2}\, V_{in} = \sqrt{2} \times 20 = 28.28V \rightarrow$ Peak output voltage (Peak input voltage)

Wkt Average Value @ DC Value,

$$V_{dc} = \frac{V_m}{\pi} = \frac{28.28}{\pi} = 9.003V \rightarrow \text{Average value @ DC value}$$

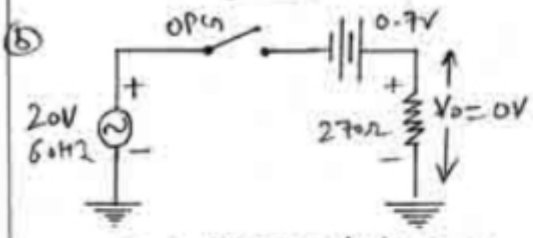
The diode conducts only for negative half cycle of input signal & the output waveform is shown in fig (*)



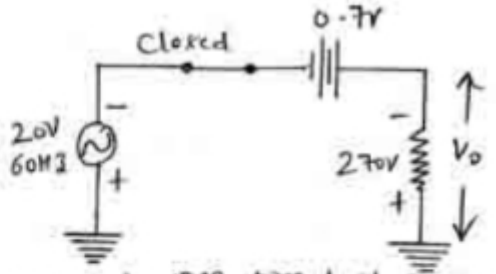
$V_{dc} = -9.003V$

Fig (a)

(b)



Circuit in positive half cycle



Circuit in negative half cycle

Applying KVL to the loop,

$-V_{in} + 0.7 + V_o = 0$

$\Rightarrow \quad V_o = V_{in} - 0.7$

$\Rightarrow \quad (V_o)_m = (V_{in})_m - 0.7$

$= \sqrt{2} \times 20 - 0.7$

$(V_o)_m = 27.58V$

Peak output voltage

Average value @ DC value

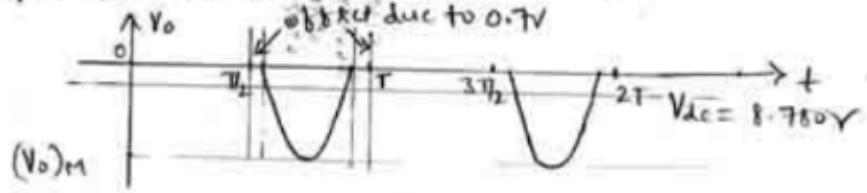
$V_{dc} = \frac{(V_o)_m}{\pi} = \frac{27.58}{\pi} = 8.780V$

Average value @ DC value

Peak load current (maximum)

$I_o = \frac{V_{in} - 0.7}{R_L} \Rightarrow I_m = \frac{(V_{in})_m - 0.7}{R_L}$

Diode doesnot conduct during positive half cycle of input signal & during negative half cycle, the diode conducts only when the input voltage is $-0.7V$. The o/p wave form is shown in fig (**)



28 A diode whose internal resistance is 20Ω, is used to supply power to a 1KΩ load from a 110V (rms) source of supply. Calculate (a) Peak load voltage (b) Peak load current (c) DC load voltage (d) DC load current (e) Peak load current (f) DC diode V/I

(h) Total input power to the circuit (i) Power delivered to the load (j) PIV (K) % Regulation (Average value of load power)

Ref: Given $R_f = 20\Omega$, $R_L = 1000\Omega$, $V_1 = 110V$ (rms)

(a) Peak load voltage (V_M)

$$V_2 = \frac{N_2}{N_1} V_1 = V_1 = 110V \quad (\text{Assume } N_1 = N_2)$$

$$V_M = \sqrt{2}\, V_2 = \sqrt{2} \times 110 = 155.56\,V$$

(b) Peak load current (I_M)

$$I_M = \frac{V_M}{R_f + R_L} = \frac{155.56}{20 + 1000}$$

$$I_M = 152.5\,mA$$

(c) DC load voltage (V_{dc})

$$V_{dc} = \frac{V_M/\pi}{1 + R_f/R_L} = \frac{155.56/\pi}{1 + 20/1000}$$

$$V_{dc} = 48.54\,V$$

(d) DC load current (I_{dc})

$$I_{dc} = \frac{I_m}{\pi} = \frac{152.5 \times 10^{-3}}{\pi}$$

$$I_{dc} = 48.54\,mA$$

(e) AC load voltage (RMS load voltage) (V_{rms})

$$V_{rms} = \frac{V_M/2}{1 + R_f/R_L} = \frac{155.56/2}{1 + 20/1000}$$

$$= 76.25\,V$$

(f) RMS load current (AC load current) (I_{rms})

$$I_{rms} = I_m/2 = 76.25\,mA$$

(g) DC diode voltage (V_{dc}')

$$V_{dc}' = -V_{dc}$$

$$V_{dc}' = -48.54\,V$$

(h) Total input power to the circuit (P_{in})

$$P_{in} = I_{rms}^2 (R_f + R_L)$$

$$P_{in} = 5.93W$$

(i) Power delivered to load (P_{dc})

$$P_{dc} = \frac{V_{dc}^2}{R_L} \text{ (or) } I_{dc}^2 R_L = \frac{(48.54)^2}{1000}$$

$$P_{dc} = 2.356W$$

(j) PIV (PIV)

$$PIV = V_M$$

$$PIV = 155.56\,V$$

(k) % Regulation

$$\% \text{ Regulation} = \frac{R_f}{R_L} \times 100 = \frac{20}{1000} \times 100 = \underline{2}$$

(29) The input to a half-wave rectifier is given through a 10:1 transformer from a supply given by $230 \sin 314t$ V. If $R_f = 50\Omega$ & $R_L = 500\Omega$, determine (a) DC load voltage (b) maximum load voltage (c) Peak load current (d) Rms load voltage (e) PIV across the diode (f) Rectification efficiency (g) DC power delivered to the load (h) Frequency of the input & output voltage.

Sol: Given, $N_1 : N_2 = 10 : 1$, $V_1 = 230 \sin 314t$ V,

$R_f = 50\Omega$, $R_L = 500\Omega$,

$$V_2 = \frac{N_2}{N_1} V_1 = \frac{1}{10} 230 \sin 314t \text{ V}$$

$$V_2 = 23 \sin 314t \text{ V}$$

Comparing with $V_2 = V_M \sin \omega t$ V

$\therefore V_M = 23$V, $\omega = 314$

$2\pi f = 314$

$$f = \frac{314}{2\pi} = 50\text{Hz}$$

(a) V_{dc}

$$V_{dc} = \frac{V_M/\pi}{1 + R_f/R_L}$$

$$= \frac{23/\pi}{1 + 50/500}$$

$V_{dc} = \underline{6.66\text{V}}$

(b) V_M

$V_M = 23$V

(c) $I_M = \frac{V_M}{R_f + R_L}$

$= \frac{23}{50 + 500}$

$I_M = \underline{0.0418\text{ A}}$

(d) V_{rms}

$$V_{rms} = \frac{V_M/2}{1 + R_f/R_L}$$

$$= \frac{23/2}{1 + 50/500}$$

$= \underline{10.45\text{V}}$

(e) PIV

$PIV = V_M$

$PIV = 23$V

(f) $\eta\%$

$$\eta\% = \frac{40.6}{1 + R_f/R_L}$$

$$= \frac{40.6}{1 + 50/500}$$

$\eta = \underline{36.91\%}$

(g) P_{dc}

$P_{dc} = I_{dc}^2 R_L$ (or) V_{dc}^2/R_L

$= 6.66^2/500 = 88.7$ mW

(h) f_{in} & f_{out}

Wkt $f_{out} = f_{in} = f = 50$Hz

(30) A half wave rectifier is used to supply 50V d.c to a resistive load of 800Ω. The diode has a resistance of 25Ω calculate a.c voltage required.

Sol: Given $V_{dc} = 50V$, $R_L = 800\Omega$, $R_f = 25\Omega$

W.K.T $$V_{dc} = \frac{V_m/\pi}{1 + R_f/R_L}$$

$$\Rightarrow V_m = V_{dc} \times \pi \times (1 + R_f/R_L) = 161.988V$$

A.C voltage of maximum value 161.988 V is required

(31) A half wave rectifier circuit is supplied from a 230V, 50Hz supply with a 3:1 transformer. The diode forward resistance is 50Ω, load resistance is 1KΩ & transformer secondary ~~resistance~~ resistance is 10Ω. Calculate peak load current & AC power to the circuit.

Sol: Given, $V_1 = 230V$, $N_1 : N_2 = 3:1$, $R_f = 50\Omega$, $R_L = 1000\Omega$, $R_s = 10\Omega$, $I_m = ?$, $P_{in} = ?$

$$V_2 = \frac{N_2}{N_1} V_1$$

$$= \frac{1}{3} 230$$

$$V_2 = 76.66V$$

$$\therefore V_m = \sqrt{2} \times V_2 = \sqrt{2} \times 76.66$$

$$V_m = 108.42V$$

I_m

$$I_m = \frac{V_m}{R_s + R_f + R_L}$$

$$= \frac{108.42}{10 + 50 + 1000}$$

$$= 102.28 mA$$

P_{in}

$$P_{in} = I_{rms}^2 (R_s + R_f + R_L)$$

$$= (51.14 \times 10^{-3})^2 [10 + 50 + 1000]$$

$$P_{in} = 2.772W$$

$$I_{rms} = \frac{I_m}{2}$$

$$= \frac{102.28 \times 10^{-3}}{2}$$

$$= 51.14 mA$$

(32) The applied input a.c power to a half-wave rectifier is 100 watts. The d.c output power obtained is 40 watts.
(i) What is the rectification efficiency?
(ii) What happens to remaining 60 watts?

Sol:

(i) $\eta = \frac{\text{D.C output Power}}{\text{A.C input Power}} = \frac{40}{100} = 40\%$

(ii) 40% Efficiency of rectification doesnot mean that 60% of power is lost in the rectifier circuit. In fact, a crystal diode consumes little power due to its small internal resistance. The 100W a.c power is contained as 50watts in positive half cycles and 50watts in negative half-cycles. The 50W in the negative half-cycles are not supplied at all. Only 50watts in the positive half-cycles are converted into 40watts.

$\therefore$ Power efficiency $= \frac{40}{50} \times 100 = 80\%$.

$\therefore$ Efficiency of rectification is 40% & not 80%. (which is Power efficiency)

(33) In a FWR, the forward resistance of the diode is 10Ω, the load resistance is 2kΩ. The secondary voltage with reference to center tap is 220 V. Calculate
(a) Peak load voltage (b) Peak load voltage (c) RMS load voltage (d) RMS load current (e) DC load voltage (f) DC load current (g) DC current in each diode (h) DC output power (i) Percentage regulation (j) PIV across each diode (k) RMS current through each diode

Sol: Given $R_f = 10\Omega$, $R_L = 2k\Omega$, $V_2 = 220V$ (rms)

(a) Peak load Voltage (V_M)

$V_M = \sqrt{2}\, V_2 = \sqrt{2} \times 220 = 311.12\,V$

(b) I_m

$I_m = \frac{V_m}{R_f + R_L}$

$I_m = \frac{311.12}{10 + 2000}$

$I_m = 0.154\,A$

@

$154.78\,mA$

(c) I_{rms}

$I_{rms} = \frac{I_m}{\sqrt{2}}$

$= \frac{154.78 \times 10^{-3}}{\sqrt{2}}$

$= 109.45\,mA$

(d) V_{rms}

$V_{rms} = \frac{V_m}{\sqrt{2}}$

$= \frac{311.12}{\sqrt{2}}$

$V_{rms} = 219.99\,V$

(e) $V_{dc} = \frac{2V_m/\pi}{1 + R_f/R_L}$

$= \frac{2 \times 311.12/\pi}{1 + 10/2000}$

$= 197.07\,V$

(f) $I_{dc} = \frac{2I_m}{\pi}$

$= \frac{2 \times 154.78 \times 10^{-3}}{\pi}$

$= 98.53\,mA$

(g) Since each diode acts as HWR, the dc current through each diode is,

$I_{dc(diode)} = \frac{I_m}{\pi}$

$= \frac{154.78 \times 10^{-3}}{\pi}$

$= 49.26\,mA$

(h) $P_{dc} = I_{dc}^2 R_L$

@ $= \frac{V_{dc}^2}{R_L}$

$= \frac{(197.07)^2}{2000}$

$= 19.41\,W$

(i) % Regulation $= \frac{R_f}{R_L} \times 100$

$= \frac{10}{2000} \times 100$

$= 0.5\%$

(j) $PIV = 2V_m$

$= 2 \times 311.12$

$= 622.24\,V$

(k) Since each diode acts as HWR, the RMS current through each diode is,

$I_{rms(diode)} = \frac{I_m}{2} = \frac{154.78 \times 10^{-3}}{2} = 77.39\,mA$

39) The center-tap FWR has a load of 2kΩ, the forward resistance of the diode is 10Ω. The ac voltage applied to the diodes is 200V-0-200V. Calculate

(a) Average load current (b) Average load voltage

(c) ripple ~~factor~~ (d) Efficiency (e) ripple voltage

(f) if a capacitor of 25MF is connected across the load

Sol: Given, $R_L = 2K\Omega$, $R_f = 10\Omega$, $V_2 = 200V$

$C = 25MF$

$\Rightarrow V_m = \sqrt{2}V_2 = \sqrt{2} \times 200$

$V_m = 282.84V$

(a) $I_{dc} = \frac{2I_m}{\pi}$

$= \frac{2 \times 140.71 \times 10^{-3}}{\pi}$

$= 89.57mA$

(b) $V_{dc} = I_{dc} R_L$

$= 89.57 \times 10^{-3} \times 2000$

$= 179.15V$

$I_m = \frac{V_m}{R_f + R_L}$

$= \frac{282.84}{10 + 2000}$

$= 140.71mA$

(c) $\gamma = \frac{V_{ac}}{V_{dc}}$

$\Rightarrow V_{ac} = \gamma V_{dc}$

$= 0.483 \times 179.15$ ($\because \gamma = 0.483$ for FWR)

$V_{ac} = 86.53V$

(d) $\eta = \frac{81.2\%}{1 + R_f/R_L}$

$= \frac{81.2\%}{1 + 10/2000}$

$= 80.79\%$

(e) If capacitor is connected across the load, then

Ripple factor $\gamma = \frac{1}{4\sqrt{3} f R_L C} = \frac{1}{4\sqrt{3} \times 50 \times 2000 \times 25 \times 10^{-6}} = 0.0577$

Let $f = 50Hz$

New ripple Voltage,

$V_{ac} = \gamma V_{dc}$

$= \gamma \left(V_m - \frac{I_{dc}}{4fC}\right)$

$= 0.0577 \left(282.84 - \frac{89.57 \times 10^{-3}}{4 \times 50 \times 25 \times 10^{-6}}\right)$

$= 15.28V$

[Later FWR, $V_m = V_m - \frac{I_{dc}}{4fC} @ \frac{V_m}{1 + \frac{1}{4fCR_L}}$]

35) What is AC input power from the transformer secondary used in FWR to deliver 100W of DC power to the load?

Sol: W.K.T $\eta = \frac{P_{dc}}{P_{ac}} \times 100$

$\Rightarrow P_{ac} = \frac{P_{dc}}{\eta} \times 100$

$= \frac{100}{81.2} \times 100$ ($\because \eta = 81.2\%$ for FWR)

$P_{ac} = 123.15W$

36) In the centre-tap circuit shown in fig (36), Find

(i) DC output voltage
(ii) PIV
(iii) Rectification efficiency
(iv) Frequency of output waveform

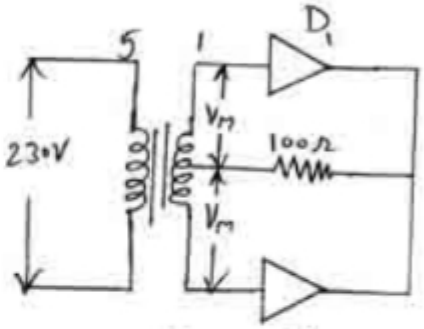


Fig (36)

Sol: Given $N_1 : N_2 = 5 : 1$, $V_1 = 230V$, $R_L = 100\Omega$

W.K.T $V_2 = \frac{N_2}{N_1} V_1 = \frac{1}{5} 230 = 46V$

Maximum voltage across secondary $= \sqrt{2} V_2 = \sqrt{2}\, 46 = 65.05V$

∴ Maximum voltage across half secondary winding is,

$V_m = \frac{65.05}{2} = 32.52V$

(i) $V_{dc} = \frac{2V_m}{\pi} = 20.70V$ ($\because R_f = 0$)
$1 + R_f/R_L$

(ii) $PIV = 2V_m = 2 \times 32.52 = 65.05V$

(iii) $\eta = \frac{81.2\%}{1 + R_f/R_L} = 81.2\%$ ($\because R_f = 0$)

(iv) $f_{out} = 2 f_{in} = 2 \times 50 = 100Hz$ (Ckt $f_{in} = 50Hz$)

(37) If ac supply voltage is $220\sin 314t$ V (for FWR) find maximum voltage across secondary winding, for 10:1 turns ratio

Sol Given $N_1 : N_2 = 10:1$ $\quad V_1 = 220\sin 314t$ V

$$V_2 = \frac{N_2}{N_1} V_1 = \frac{1}{10} 220\sin 314t$$

$$V_2 = 22\sin 314t \quad (V_2 = V_m \sin \omega t)$$

$\Rightarrow$ Maximum voltage across secondary $= 22$ V

$\therefore$ Maximum voltage across secondary winding $= \frac{22}{2} = 11$V

(38) A full wave bridge rectifier uses transformer secondary voltage of $100\sin \omega t$ V. The forward resistance of each diode is 25Ω & load resistance is 950Ω. Calculate (i) DC output voltage (ii) DC value of current through R_L (iii) PIV across non-conducting diode. (iv) Percentage regulation (v) Peak diode current (Peak load current) (vi) DC current through each diode (vii) RMS current through each diode

Sol Given, $V_2 = 100\sin \omega t$ V, $R_f = 25\Omega$, $R_L = 950\Omega$

$\Rightarrow V_m = 100$

(i) $V_{dc} = \dfrac{2V_m/\pi}{1 + 2R_f/R_L}$

$= \dfrac{2\times 100/\pi}{1 + 2\times 25/950}$

$= 60.48$V

(ii) $I_{dc} = \dfrac{2I_m}{\pi}$

$= \dfrac{2\times 100\times 10^{-3}}{\pi}$

$= 63.66$mA

(iii) PIV $= V_m$

$= 100$V

(iv) % Regulation $= \dfrac{2R_f}{R_L} \times 100$

$= 5.26\%$

(v) $I_m = \dfrac{V_m}{2R_f + R_L}$

$= \dfrac{100}{2\times 25 + 950}$

$= 100$mA

(vi) $I_{dc}(\text{diode}) = \dfrac{I_{dc}}{2} = \dfrac{I_m/\pi}{2}$

$= 31.83$mA

(viii) $I_{rms(diode)} = \frac{I_m}{2} = \frac{100mA}{2} = \underline{50mA}$

(Each diode acts as HWR)

(39) A FW bridge rectifier uses four diodes & a transformer of ratio of 230V : 110V. The forward resistance of each diode is 25Ω & load resistance is 500Ω. find Maximum value of current in the circuit

Sol

Peak value of Secondary Vtg,

$$V_M = \sqrt{2} \times 110 = \underline{155.56V}$$

Maximum value of current in the circuit,

$$I_m = \frac{V_m}{2R_f + R_L} = \frac{155.56}{2 \times 25 + 500} = \underline{282.8mA}$$

(40) A bridge rectifier consisting of 4 identical diodes produces a direct current of 124.49mA across a 2kΩ resistive load. If the rms value of Primary input supply is 220V, Calculate the Primary to Secondary ratio of the transformer if each diode has a forward resistance of 10Ω.

Sol

Given $I_{dc} = 124.49mA$, $R_L = 2k\Omega$, $V_1 = 220V$, $R_f = 10\Omega$

We have, $I_{dc} = \frac{2I_m}{\pi}$

$$\Rightarrow I_m = \frac{\pi I_{dc}}{2} = \frac{\pi \times 124.49 \times 10^{-3}}{2} = \underline{0.195A}$$

& We get $V_m = I_m(2R_f + R_L) = 0.195(2 \times 10 + 2000) = \underline{393.9V}$

Also we have, $V_m = \sqrt{2}\, V_2$

$$\Rightarrow V_2 = \frac{V_m}{\sqrt{2}} = \frac{393.9}{\sqrt{2}} = \underline{278.5V}$$

Now, $V_2/V_1 = N_2/N_1$

$$\Rightarrow \frac{N_2}{N_1} = \frac{279.5}{220} = 1.26$$

$$\Rightarrow N_1 : N_2 = 1 : 1.26$$

(11) A bridge rectifier is driving a load resistance of 100Ω. It is driven by a source voltage of 230V, 50Hz. Neglecting diode resistances, Calculate
(a) frequencies of output waveform. (b) Average output V/g

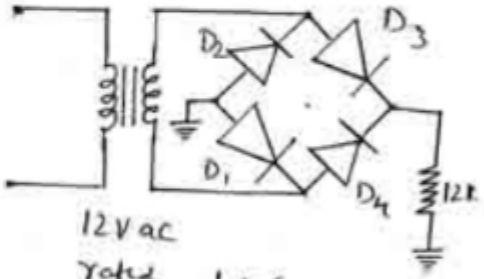
Sol: Given $V_2 = 230V$, $f = 50Hz$. $R_L = 100\Omega$.

$V_m = \sqrt{2} V_2 = 141.42 V$

(a) $f_{out} = 2f = 100Hz$

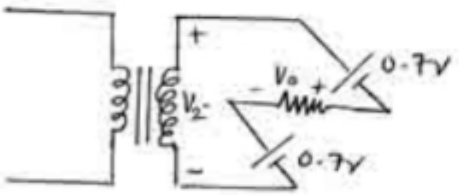
(b) $V_{dc} = \frac{2V_m/\pi}{1 + 2R_f/R_L} = \frac{2 \times 141.42/\pi}{1 + 2(0)/100} = 90.03V$

(12) The bridge rectifier is shown in fig(12) (use Si diodes). Find
(i) DC o/p V/g (ii) DC o/p current
(iii) Sketch the o/p V/g



fig(12)

Sol:



KVL

$$V_2 - 0.7 - V_o - 0.7 = 0$$

$$\Rightarrow V_o = V_2 - 1.4$$

$$\Rightarrow (V_o)_m = (V_2)_m - 1.4$$

$$= 16.97 - 1.4$$

$(V_o)_m = 15.57V$ → Peak output voltage

Given $R_L = 12k\Omega$

$V_2 = 12V$

$V_m = \sqrt{2} V_2 = 16.97V$

(i) DC @ Average o/p V/g

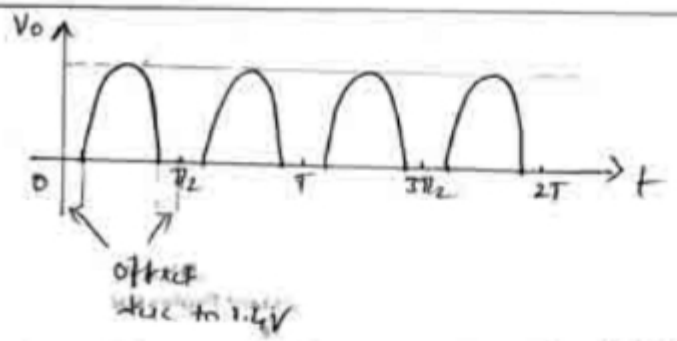
$$V_{dc} = \frac{2(V_o)_m}{\pi} = \frac{2 \times 15.57}{\pi}$$

$V_{dc} = 9.91V$

(ii) Average @ DC o/p current

$$I_{dc} = \frac{V_{dc}}{R_L} = 825.8\,mA$$

(iii)



(13) A HWR with capacitor filter is supplying a resistive load of 1000Ω. The value of filter capacitor is 200MF. If the supply voltage to the rectifier is 200V at 50Hz. Calculate (a) Ripple factor (b) DC output voltage (c) DC load current (d) PIV across the diode (e) RMS ripple output voltage

Sol:

Given, $R_L = 1000\,\Omega$, $C = 200\mu F$, $V_2 = 220V$

$f = 50Hz$ $\qquad V_m = 220\sqrt{2} = 311.13V$

(a) $\gamma = \frac{1}{2\sqrt{3} f R_L C}$

$= \frac{1}{2\sqrt{3} \times 50 \times 1000 \times 200 \times 10^{-6}}$

$= 0.0288$ (a) ~~28.8%~~

$= 2.88\%$

(b) $V_{dc} = V_m - \frac{I_{dc}}{2fC}$

$V_{dc} \overset{(a)}{=} \frac{V_m}{1 + \frac{1}{2fCR_L}}$

$= \frac{311.13}{1 + \frac{1}{2 \times 50 \times 200 \times 10^{-6} \times 1000}}$

$= 296.31V$

(c) $I_{dc} = \frac{V_{dc}}{R_L}$

$= \frac{296.31}{1000}$

$= 0.296A$

(d) $PIV = V_m$

$= 311.13V$

(e) $V_{ac} = \gamma V_{dc} \left(\because \gamma = \frac{V_{ac}}{V_{dc}}\right)$

$\Rightarrow V_{ac} = 0.0288 \times 296.31$

$V_{ac} = 8.533V$

(14) In a FWR with a capacitor filter, the load current from the circuit operating from 230V, 50Hz supply is 10mA. Estimate the value of capacitor required to keep the ripple factor less than 1%. Also find the minimum value of capacitance

Sol: Given. $V_2 = 230V$, $f = 50Hz$, $I_{dc} = 10mA$, $C = ?$

$\gamma < 0.01$ @ 1%

$V_m = \sqrt{2}\, V_2$

$= \sqrt{2}\, 230$

$= 325.269V$

We know $\gamma = \frac{1}{4\sqrt{3} f R_L C} < 0.01$

We know $R_L = \frac{V_{dc}}{I_{dc}}$

$R_L = \frac{V_m}{I_{dc}}$ ($\because V_{dc} \simeq V_m$)

$= \frac{325.269}{10 \times 10^{-3}}$

$= 32.5269 k\Omega$

$\Rightarrow \frac{1}{C} < 0.01 \times 4\sqrt{3} \times 50 \times 32.52 \times 10^3$

$\Rightarrow C > \frac{1}{0.01 \times 4\sqrt{3} \times 50 \times 32.52 \times 10^3}$

$C > 8.87 \mu F$

$C_{min} = 8.87 \mu F \rightarrow$ Minimum Value

(15) A FW bridge rectifier supplies a load of 400Ω in parallel with a capacitor of 500 μF. If the ac supply voltage is $230 \sin 314t$ (V), find @ Ripple factor.

(b) DC load current.

Sol: Given $R_L = 400\Omega$, $C = 500 \mu F$. $V_2 = V_1 = 230 \sin 314t$

$\Rightarrow V_m = 230V$

$\omega = 314$

$f = \frac{314}{2\pi} = 50Hz$

(a) $\gamma = \frac{1}{4\sqrt{3} f R_L C} = \frac{1}{4\sqrt{3} \times 50 \times 400 \times 500 \times 10^{-6}}$

$\gamma = 0.0144$ @ 1.44%

(b) $V_{dc} = \frac{V_m}{1 + \frac{1}{4\sqrt{3} f R_L C}} = \frac{230}{1 + \frac{1}{4\sqrt{3} \times 50 \times 400 \times 500 \times 10^{-6}}} = 224.39V$

$\therefore I_{dc} = \frac{V_{dc}}{R_L}$

$$I_{dc} = \frac{224.39}{400} = 0.56A$$

(46) A HWR dc power supply has to supply 20V to a 500Ω load. The Peak-Peak voltage should not exceed 10% of the average output voltage and the ac input frequency is 60Hz. Calculate the required capacitor value.

Sol: Given $V_2 = 20V$ $R_L = 500\Omega$

$V_m = \sqrt{2} \times 20 = 28.28V$, $f = 60Hz$, $V_{r(P-P)} = 10\%$ of V_{dc}

$C = ?$

Consider, $V_{r(P-P)} = 10\%$ of V_{dc}

$\Rightarrow V_{r(P-P)} = 0.1 V_{dc}$

$\Rightarrow 2\sqrt{3} V_{ac} = 0.1 V_{dc}$ $\left(\because V_{r(P-P)} = 2\sqrt{3} V_{ac}\right)$

$\Rightarrow \frac{V_{ac}}{V_{dc}} = \frac{0.1}{2\sqrt{3}} = 0.02$

$\Rightarrow \gamma = 0.02886$

Let $\gamma = \frac{1}{2\sqrt{3} f R_L C}$

$$C = \frac{1}{2\sqrt{3}\gamma f R_L} = \frac{1}{2\sqrt{3} \times 0.02886 \times 60 \times 500} = 343.66\mu F$$

(47) A 12V reference source is to use a series-connected Zener diode & resistor connected to a 30V supply. Select suitable components & Calculate the circuit current when the supply voltage drops to 25V.

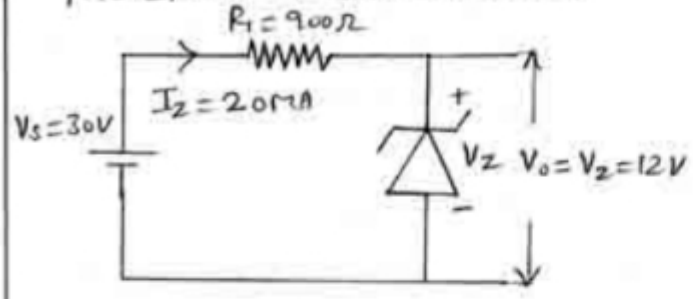
Sol: (a) Given $V_S = 30V$, $V_o = V_Z = 12V$, (b) $V_S = 25V$ $I_Z = ?$

(c) Let $I_Z = I_{ZT} = 20mA$

We have,

$$R_1 = \frac{V_S - V_Z}{I_Z} = \frac{30-12}{20\times10^{-3}} = 900\,\Omega$$

The circuit is shown below



(b) We have

$$I_Z = \frac{V_S - V_Z}{R_1} = \frac{25-12}{900} = 14.44\,mA$$

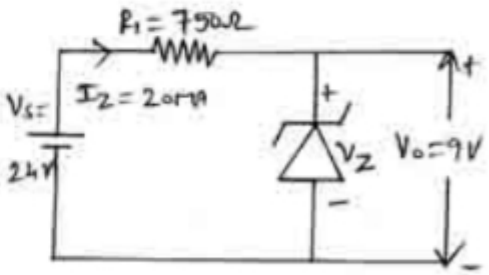
(18) Design a 9V dc reference source consisting of a Zener diode & series connected resistor to operate from a 24V supply. Determine the effect on the diode current when the supply voltage drops to 20V. & power dissipation in resistor.

Sol: (a) Given, $V_S = 24V$, $V_o = V_Z = 9V$, (b) $I_Z = ?$, $V_S = 20V$.

Let $I_Z = I_{ZT} = 20mA$. $P_{R_1} = ?$

(a) We have

$$R_1 = \frac{V_S - V_Z}{I_Z} = \frac{24-9}{20\times10^{-3}} = 750\,\Omega$$



(b) Like

$$I_Z = \frac{V_S - V_Z}{R_1} = \frac{20-9}{750} = 14.66\,mA$$

$$P_{R_1} = (I_Z)^2 R_1 = (20\times10^{-3})^2(750) = 0.3\,W$$

(19) A Zener diode has a breakdown voltage of 10V. It is supplied from a voltage source varying between 20 & 40V

in series with a resistance of 820Ω. Using an ideal zener diode model obtain minimum & maximum zener current.

Sol: Given. $V_Z = 10V$, $R_1 = 820\Omega$, $V_S = 20V - 40V$

$V_{Smin} = 20V$, $V_{Smax} = 40V$

We have, $I_Z = \frac{V_S - V_Z}{R_1}$

When $V_S = V_{Smin}$, $I_Z = I_{Zmin}$

$$I_{Zmin} = \frac{V_{Smin} - V_Z}{R_1}$$

$$= \frac{20 - 10}{820}$$

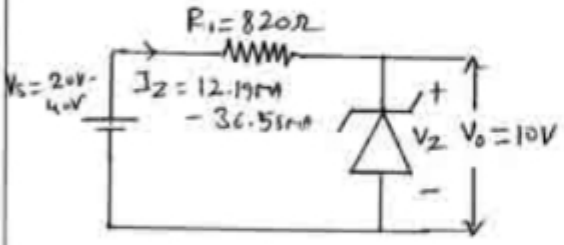
$$= 12.19mA$$

When $V_S = V_{Smax}$, $I_Z = I_{Zmax}$

$$I_{Zmax} = \frac{V_{Smax} - V_Z}{R_1}$$

$$= \frac{40 - 10}{820}$$

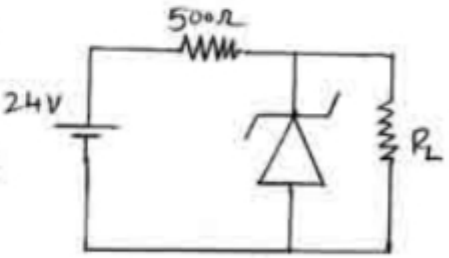
$$= 36.58mA$$



(b) Determine the minimum & maximum values of load current for which the zener diode shunt regulator shown in fig (5a) will maintain regulation

(c) What is the minimum R_L

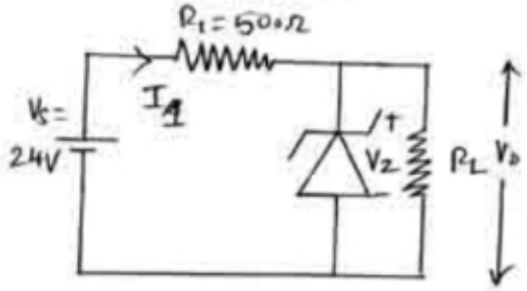
Given $V_Z = 12V$, $I_{Zmin} = 3mA$, $I_{Zmax} = 90mA$, $r_Z = 0$ Fig (5a)



Sol: Minimum load current

We have $I_1 = \frac{V_S - V_Z}{R_1} = \frac{24 - 12}{500}$

$I_1 = 24mA$



Since $I_1 << I_{Zmax}$,

$I_{Lmin} = 0$

Maximum load current

$$I_{L(max)} = I_1 - I_{Z min} = 24 - 3 = 21\,mA$$

minimum load resistance

$$R_{L min} = \frac{V_Z}{I_{L max}} = \frac{12}{21 \times 10^{-3}} = 571\,\Omega$$

51) For a Zener shunt regulator if $V_Z = 10V$, $R_S = 1k\Omega$, $R_L = 2k\Omega$, & the input varies from 22 to 40V, find the maximum & minimum values of Zener current.

Sol: Given, $V_Z = 10V$, $R_S = 1k\Omega$, $R_L = 2k\Omega$, $V_{S min} = 22V$, $V_{S max} = 40V$.

We get $I_L = \frac{V_Z}{R_L} = \frac{10}{2 \times 10^3} = 5\,mA$ (Assume $I_L = I_{L max}$ & $I_{L min} = 0$)

Maximum Zener current:

$$I_{Z(max)} = \frac{V_{S max} - V_Z}{R_S} - I_{L min} = \frac{40 - 10}{1 \times 10^3} = 30\,mA$$

Minimum Zener current

$$I_{Z(min)} = \frac{V_{S min} - V_Z}{R_S} - I_{L max} = \frac{22 - 10}{1 \times 10^3} - 5 \times 10^{-3} = 7\,mA$$

52) Design a Zener voltage regulator for $V_o = 5V$, $V_{in} = 12 \pm 3V$, $I_L = 20mA$, $P_Z = 500mW$ (Zener wattage), $I_{Z min} = 5 \times 10^{-3}$

Sol: Given $V_o = V_Z = 5V$, $V_{in min} = 12 - 3 = 9V$, $V_{in max} = 12 + 3 = 15V$.

$P_Z = 500mW$. Assume $I_{L min} = 0$, $I_{L max} = 20mA$

Ans $I_{Z max} = \frac{P_{Z max}}{V_Z} = \frac{500 \times 10^{-3}}{5} = 100\,mA$ ($P_{Z max} = P_Z$)

$R_{1 min}$ $R_{1 min} = \frac{V_{in max} - V_Z}{I_{Z max} + I_{L min}} = \frac{15 - 5}{100 \times 10^{-3} + 0} = 100\,\Omega$

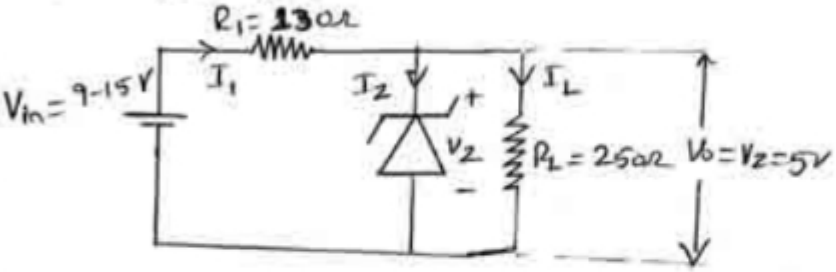
R_{1min}: $R_{1max} = \dfrac{V_{in\,min} - V_Z}{I_{Zmin} + I_{Lmax}} = \dfrac{9-5}{5\times10^{-3} + 20\times10^{-3}} = 160\Omega$

Let $R_1 = \dfrac{R_{1min} + R_{1max}}{2} = \dfrac{100+160}{2} = 130\Omega$

R_L

Now $R_L = \dfrac{V_o}{I_L} = \dfrac{5}{20\times10^{-3}} = 250\Omega$

Voltage Regulator is shown below



(33) Design a 6V dc reference source to operate from a 15V supply. The circuit has to provide a maximum possible load current. Calculate the maximum load current that can be drawn from the circuit. Also find power dissipation in series resistor.

Sol: Given $V_o = V_Z = 6V$, $V_S = 15V$.

Assume $I_{ZT} = 20mA$, $P_D = 400mW$ & $I_{Zmin} = 5mA$

We have, $I_{Zm} = \dfrac{P_D}{V_Z} = \dfrac{400\times10^{-3}}{6} = 66.67mA$

Also we have, $R_1 = \dfrac{V_S - V_Z}{I_{Zm}} = \dfrac{15-6}{66.67\times10^{-3}} = 135\Omega$

Power dissipation in R_1: $P_{R_1} = (I_{Zm})^2 R_1 = (66.67\times10^{-3})^2 \times 135$

$P_{R_1} = 0.6W$

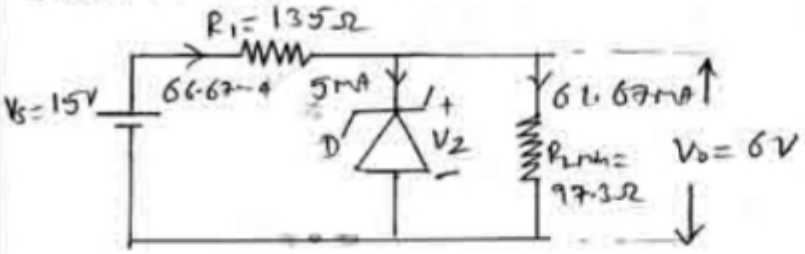
We have, $I_{Zm} = I_{Lmax} + I_{Zmin}$

$\Rightarrow I_{Lmax} = I_{Zm} - I_{Zmin} = 66.67mA - 5mA$

$I_{Lmax} = 61.67mA$ //

$$R_{Lmin} = \frac{V_o}{I_{Lmax}} = \frac{6}{61.67\times10^{-3}} = 97.3\,\Omega$$

Zener voltage regulator is shown below



(24) A 24V, 600mW Zener diode is used for providing a 24V stabilized supply to a variable load. If the input voltage is 32V, calculate the following

(i) value of series resistance (ii) Diode current when $R_L = 2.4k\Omega$

(iii) minimum R_L (iv) Power dissipated in Resistance (series)

Sol Given $V_s = 32V$, $V_o = V_z = 24V$, $P_D = 600mW$

Assume $I_{Zmin} = 5mA$

(i) $$R_1 = \frac{V_s - V_z}{I_{Zm}} = \frac{32-24}{25\times10^{-3}} = 320\,\Omega$$

$$\left[I_{Zm} = \frac{P_D}{V_z} = \frac{600\times10^{-3}}{24} \Rightarrow I_{Zm} = 25mA \right]$$

(ii) $$I_Z = I_{Zm} - I_L \quad (\because I_{Zm} = I_Z + I_L)$$

$$= 25\times10^{-3} - 10\times10^{-3} \quad \left(I_L = \frac{V_o}{R_L} = \frac{24}{2.4\times10^3} = 10mA \right)$$

$$= 15mA$$

(iii) $$R_{Lmin} = \frac{V_o}{I_{Lmax}} = \frac{24}{20\times10^{-3}} = 1200\,\Omega$$

$$\left[\because I_{Zm} = I_{Lmax} + I_{Zmin} \text{ or } I_{Lmax} = I_{Zm} - I_{Zmin} = 25\times10^{-3} - 5\times10^{-3} = 20mA \right]$$

(iv) $$P_{R_1} = (I_{Zm})^2 R_1$$

$$= (25\times10^{-3})^2 \times 320$$

$$= 0.2W$$

(5) The output voltage of a dc power supply varies from 30 V to 29.6 V when the load current is increased from zero to maximum. The voltage also increases to 30.7 V when the ac supply increase by 10%. Calculate the load & source effect. & the load & line regulation.

Sol: Given

$\Delta V_o = 30 - 29.6$ (for $\Delta I_{L(max)}$) $V_o = 30V$

$= 0.4V$ (for $\Delta I_{L(max)}$)

$\Delta V_o = 30.7 - 30$ (for 10% change in V_s)

$= 0.7V$ (for 10% change in V_s)

Load effect = ΔV_o for $\Delta I_{L(max)} = 0.4V$

Source effect = ΔV_o for 10% change in $V_s = 0.7V$

Load regulation = $\frac{\Delta V_o \text{ for } \Delta I_{L(max)}}{V_o} \times 100 = \frac{0.4}{30} \times 100 = 1.33\%$

Line regulation = $\frac{\Delta V_o \text{ for 10\% change in } V_s}{V_o} \times 100 = \frac{0.7}{30} \times 100 = 2.33\%$

Syllabus: Bipolar Junction Transistors: BJT operation, BJT Voltages and currents, BJT amplification, Common base, Common Emitter and Common Collector characteristics. Numerical examples as applicable.

Introduction:

→ The first transistor was invented in 1947 (23 Dec) at the Bell Telephone laboratories (USA) by Dr. William Shockley, Dr. John Bardeen & Dr. Walter H. Brattain.

→ Transistor is an electronic device consisting of two pn junctions formed by sandwiching either P-type or n-type semiconductor between a pair of opposite types.

→ Transistor is a three terminal (three layers) & two junctions electronic device. (2 Port device)

→ Transistor is a current controlled device (ie output current, voltage and/or power are controlled by its input current)

→ Transistor can be considered as connection of two back-to-back diodes (fig ③) & (fig ⑥)

→ The term transistor is derived from TRANSfer-reSISTOR (∵ amplification is achieved by passing input current from a region of low resistance to a region of high resistance)

→ Transistor can be used as switch and amplifier [Amplification of weak signals (current & voltage)]

→ Three blocks [(P, n, P) or (n, P, n)] are grown out of same crystal by adding corresponding impurities in turn.

→ Types of transistors (Based on number of charge carriers):

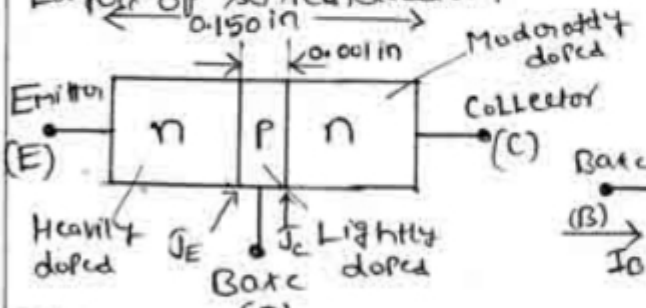
- Unipolar Junction Transistor (UJT): Current conduction is only due to one type of charge carriers [either electrons or holes (majority carriers)]
- Bipolar Junction Transistor (BJT): Current conduction is due to both the types of charge carriers [holes & electrons (majority & minority carriers)]

→ Types of Bipolar Junction transistors (Construction):

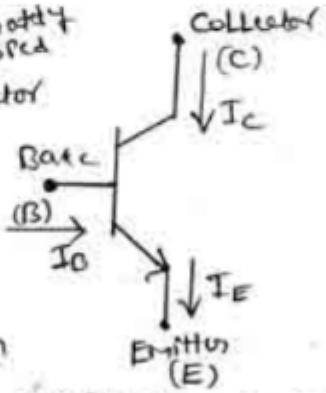
There are two types of BJTs

① npn transistor

- npn transistor is obtained when a P-type layer of semiconductor is sandwiched between two n type layers of semiconductor.



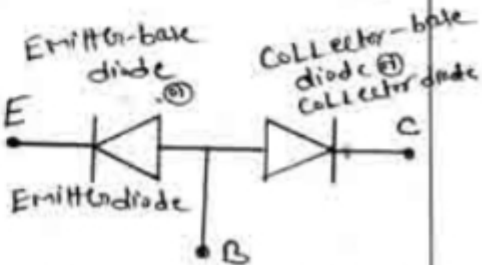
Fig①: Schematic representation of npn transistor



Fig②: Symbol of npn transistor

- There are three terminals one taken from each type of semiconductor (Emitter, Base & Collector)

~ Emitter: ⇒ The section on one side that supplies charge carriers (electrons) is called the emitter



Fig③: Two diode transistor analogy of Diode equivalent circuit of npn transistor

⇒ It is a heavily doped region
⇒ It is always forward biased w.r.t base & provides low resistance in the emitter.

~ Base: ⇒ The middle layer (or section or region) between the emitter & collector is called the base.
⇒ It is thin & lightly doped region.

~ Collector: ⇒ The section on the other side which collects charge carriers (electrons) is called the collector
⇒ It is moderately doped region & larger than emitter & base.
⇒ It is always reverse biased w.r.t base & provides high resistance in the collector.

Note: ① During transistor operation, much heat is produced at the collector junction, so collector is made larger to dissipate the heat.

- Transistor has two PN junctions (i.e it is like two diodes)

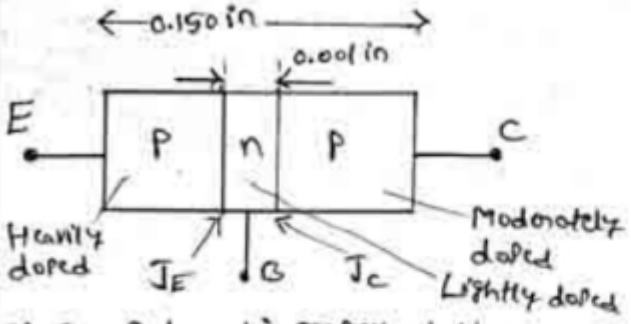
⇒ The junction between emitter & base is emitter-base junction (J_E) or emitter-base diode or emitter diode (Always FB)

⇒ The junction between the base & collector is collector-base junction (J_C) or collector-base diode or collector diode (Always RB)

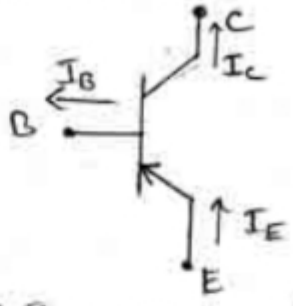
- The ratio of the total width to center layer (Base) is $0.150/0.001 = 150:1$
- The ratio of doping level of outer layers (E & C) to center layer (B) is typically 10:1 or less
- The direction of arrow head (fig ②) indicates the direction of conventional current flow in transistor.
- Free electrons are majority carriers & holes are minority carriers.

(b) PnP transistor

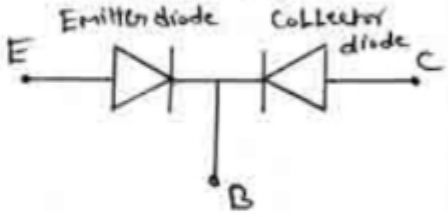
- PnP transistor is obtained by sandwiching a n-type semiconductor layer between two P-type layers of semiconductor.



Fig(4): Schematic representation of PnP transistor



Fig(5): Symbol of PnP transistor



Fig(6): Diode equivalent circuit of PnP transistor

- Emitter supplies holes to other two regions
- collector collects holes
- Holes are the majority carriers & electrons are minority carriers.

→ Transistor manufacturing techniques

Basic techniques used for transistor manufacturing techniques are

(a) Grown-junction (b) Alloy (c) Diffused-junction (d) Epitaxial.

→ Transistor Package types:

Fig(7): Transistor package types

Low Power transistors: (a), (b), (c)

Metal can-type (a), (b), (c), (e)

Plastic enclosure (d)

* **Unbiased transistor: Depletion regions & Barrier Voltages of an unbiased transistor)**

① **npn transistor:**

→ A transistor with no external dc voltage is called unbiased transistor.

→ The base layer is very thin & lightly doped compared to the outer layers.

→ The outer layers are more heavily doped than the base layer.

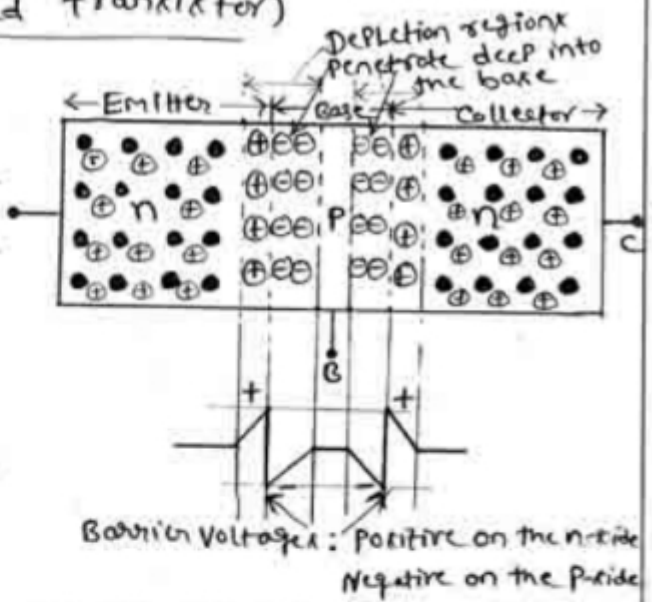


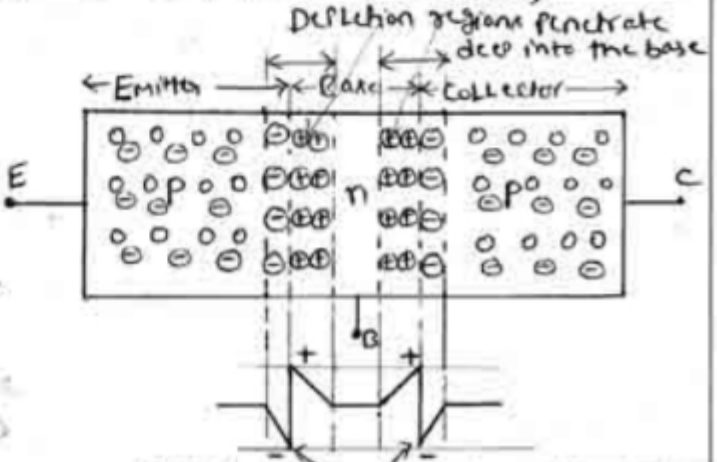
Fig ⑧: Depletion regions & barrier voltages at the junctions of an unbiased npn transistor

→ During diffusion, depletion regions penetrate more deeply into the base from either side, thus the distance between the two depletion layers within the base is reduced.

→ Junction barrier voltages are positive on the emitter & collector and negative on the base (0.3V for Ge & 0.7V for Si) (Electrons are majority carriers)

② **pnp transistor:**

Fig ⑨: Depletion regions & barrier voltages at the junctions of an unbiased pnp transistor



Explanation as same as npn circuit →

→ A PnP transistor behaves exactly like a npn transistor with the exception that the holes are majority carriers.

→ Junction barrier voltages are positive on the base and negative on the emitter & collector

---

Note:

① Modes of transistor operation ② Different ways of biasing a transistor ③ Regions of operation of BJT

④ operating regions of a transistor :

Application of suitable dc voltages across the transistor terminals is called biasing.

A transistor can be operated in four different regions

ⓐ Active region ⓑ Linear region ⓒ Forward-active region.

Ⓑ Saturation region.

ⓒ Cut-off region.

ⓓ Reverse-active region.

ⓐ Active region: (Fig 10)

→ The Emitter-base junction (J_E) is forward biased (FB) & the Collector-base junction (J_C) is reverse biased (RB).

→ For NPN transistor:

FB requires

The negative terminal of a battery is connected to N-side & positive terminal to P-side.

RB requires

The positive terminal of a

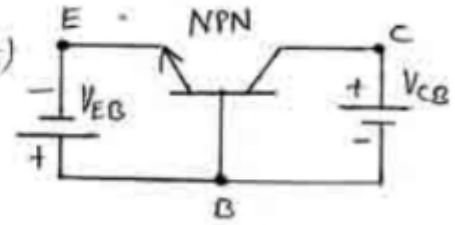


Fig 10 ⓐ Forward-active (NPN)

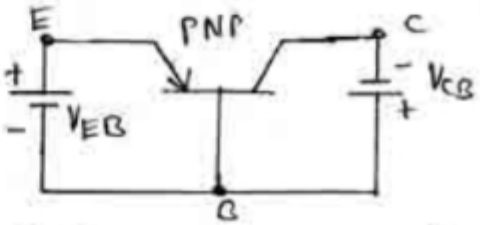


Fig 10 ⓑ: Forward-active (PNP)

battery is connected to N-side & negative terminal to P-side.

→ The collector current consists of two components:
(i) current due to the forward biasing of EB junction &
(ii) current due to reverse biasing of CB junction [I_{CO} or I_{CBO}] (Very small in magnitude)

(b) Saturation region: (Fig 11)

→ Both the Emitter-base & Collector-base junctions are forward biased

→ I_C increases rapidly for a very small change in V_{CB}.

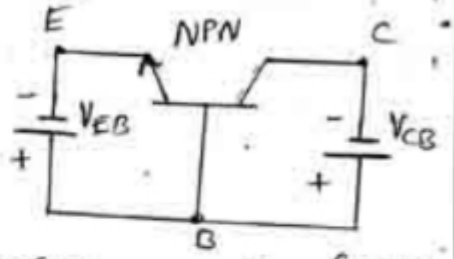


Fig (11)(a): Saturation (NPN)

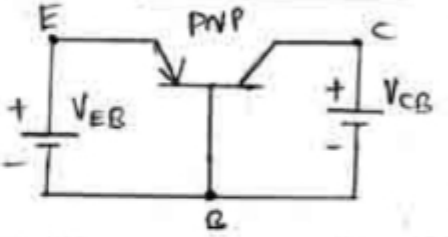


Fig (11)(b): Saturation (PNP)

(c) Cut-off region: (Fig 12)

→ Both the emitter-base & Collector-base junctions are reverse biased.

→ The current is very small & transistor is assured to be in off state.

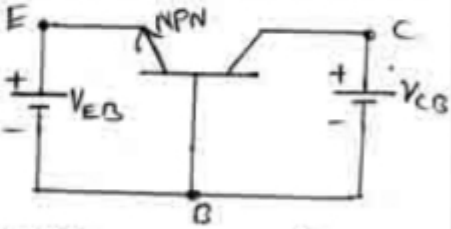


Fig (12)(a): Cut-off (NPN)

(d) Reverse-active region: (Fig 13)

→ The Emitter-base junction is reverse biased & the Collector-base junction is forward biased.

→ It is used for less amplification.

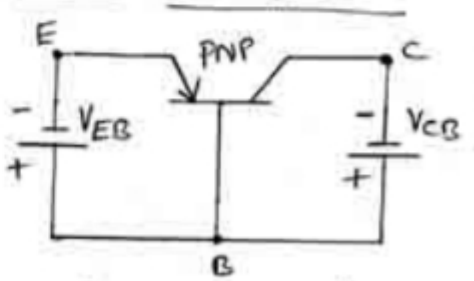


Fig (12)(b): Cut-off (PNP)

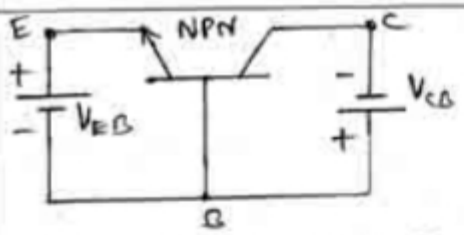


Fig 13 ⓐ : Reverse active (NPN)

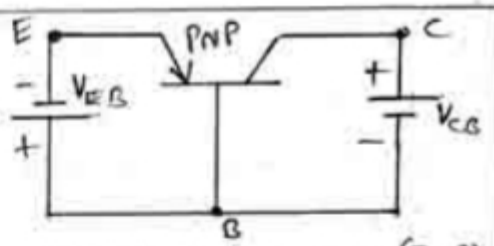


Fig 13 ⓑ : Reverse active (PNP)

Region of operation	Emitter-Base junction J_E	Collector-Base junction J_C	Application
① Active	FB	RB	Good amplification
② Saturation	FB	FB	Closed switch (ON)
③ Cut-off	RB	RB	Open switch (OFF)
④ Reverse-active	RB	FB	Less amplification

Biased transistor

① Principle of operation of transistor:

① NPN transistor:
(Principle of operation)

→ Emitter-base junction is forward biased & Collector-base junction is reverse biased.

→ The forward bias on the emitter-base junction causes the electrons in the n type emitter to flow towards the base (repelled by negative potential of V_{EB}).

This constitutes emitter current (I_E) (n→p) (opposite to flow of electrons)

→ The base is lightly doped & very thin, so only a few electrons (less than 5%) coming from the emitter

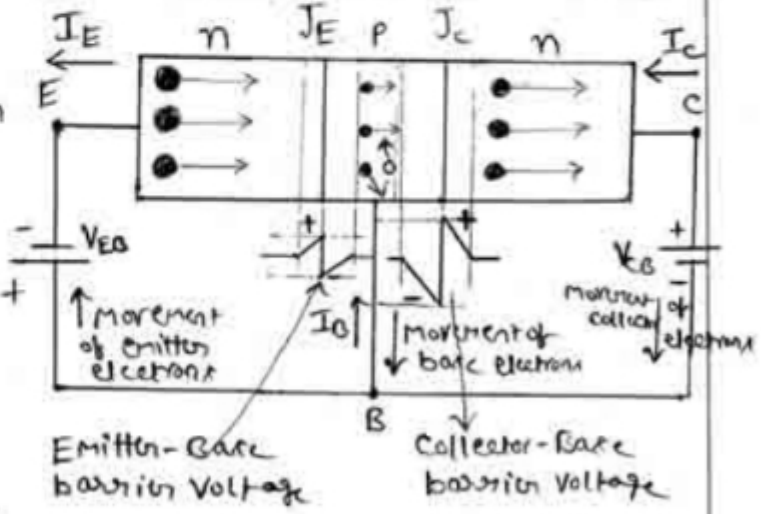


Fig (14) : operation of NPN transistor

Combine with the holes causing base current (I_B) (μA to mA)

→ The remaining electrons (more than 95%) will diffuse to the collector & constitutes collector current (or) Injected current (I_C). (mA)

→ There is another component of collector current due to thermally generated carriers. This current component (very small) is called reverse saturation current (I_{CBO}) (μA to nA)

→ It is clear that emitter current is the sum of collector & base currents

i.e $\boxed{I_E = I_B + I_C}$

Note:

① Collector current is also called as injected current because this current is produced due to electrons injected from the emitter region.

② The resistances R_E & R_C may be connected in series with emitter & collector to limit the magnitude of current in the transistor.

③ Reasons that most of the electrons from emitter continue their journey through the base to collector to form collector current are (a) The base is lightly doped & very thin. Therefore, there are a few holes which find enough time to combine with electrons (b) The reverse bias on collector is quite high & exerts attractive forces on these electrons.

④ Collector current, $I_C = \alpha I_E + I_{CBO}$

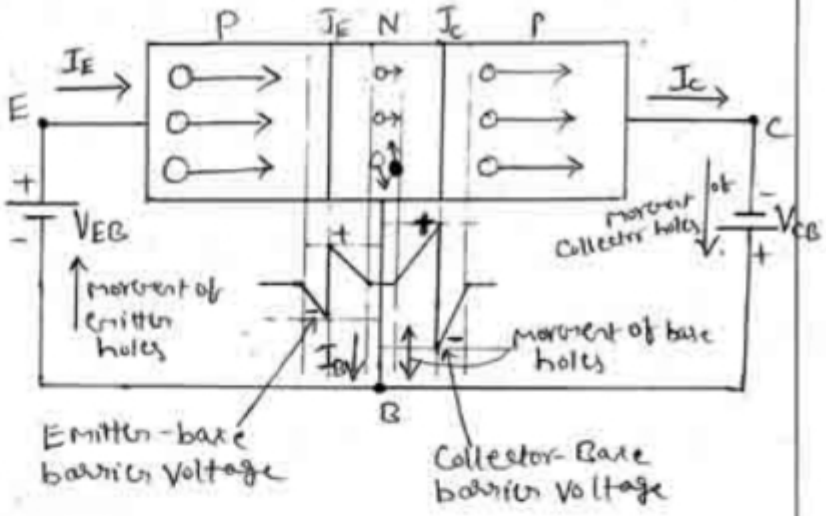
$= [(I_{C\,majority}) + (I_{C\,minority})]$ (μA to nA) → (I_C current with emitter terminal open)

(α (mA): current due to majority of electrons (more than 95%) from emitter)

(I_{CBO}: Reverse saturation current (due to thermally generated carriers) (nA) (a) minority current component Leakage current)

(2) PNP transistor:

(Principle of operation of PNP transistor)



Fig(13): Operation of PNP transistor

→ Emitter-base junction is forward biased & collector-base junction is reverse biased.

→ The forward bias on the emitter-base junction causes the holes in the emitter region to flow towards the base (repelled by positive potential of V_{EB}). This constitutes the emitter current (I_E) (mA)

→ The base is lightly doped & very thin, so only a few holes (less than 5%) coming from the emitter combine with the electrons causing base current (I_B) (μA or mA)

→ The remaining electrons (more than 95%) will diffuse to the collector & constitutes collector current or injected current (I_C) (mA)

→ There is another component of collector current due to thermally generated carriers. This current component (very small) is called reverse saturation current (I_{CBO}) (nA or μA)

→ It is clear that the emitter current is the sum of collector & base currents.

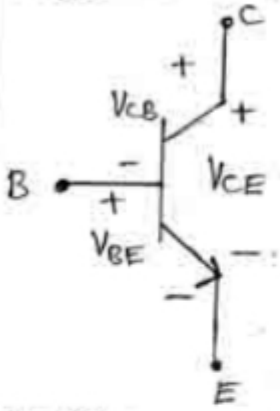
ie $\boxed{I_E = I_B + I_C}$

* BJT Voltages and Currents:

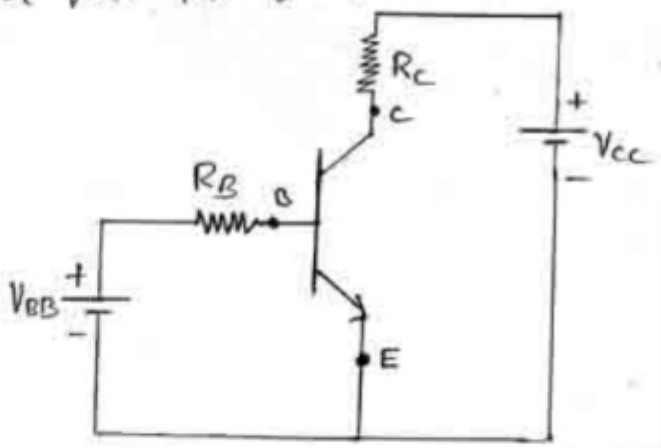
① BJT Voltages (Terminal Voltages):

② NPN transistor:

Fig⑯ shows the terminal voltages for NPN transistor.



Fig⑯ : Terminal Voltages



Fig⑰: Voltage source connection

For NPN transistor,

→ Base voltage must be positive w.r.t the emitter.

→ Collector voltage must be positive w.r.t the base.

→ Collector voltage must be positive w.r.t the emitter

Fig⑰ shows voltage source connection to NPN transistor via resistors.

→ Base bias voltage (V_{BB}) is connected via resistor (R_B) & the collector supply (V_{CC}) is connected via resistor (R_C).

→ The negative terminals of V_{BB} & V_{CC} are connected at the transistor emitter terminal.

→ To ensure reverse biasing of collector-base junction, V_{CC} must be much larger than V_{BB}.

→ Typical voltages: $V_{CE} = 0.3V$ for Ge & $0.7V$ for Si

$V_{CE} = 3V$ to $20V$

⑥ For PNP transistor

Fig ⑱ shows the terminal voltages for PNP transistor.

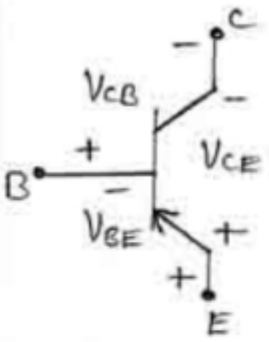


Fig ⑱: Terminal Voltages

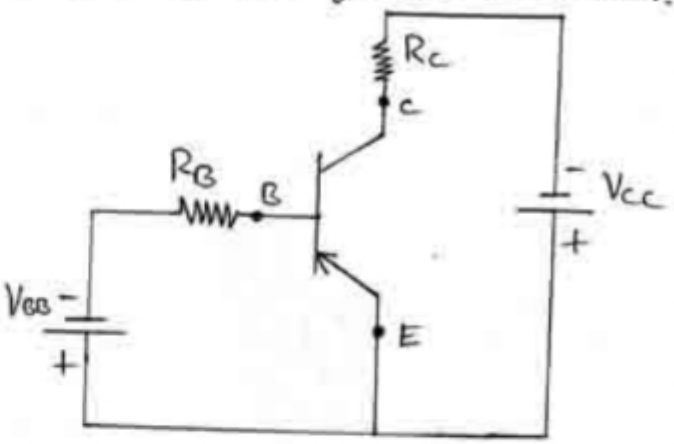


Fig ⑲: Voltage source connections

For PNP transistor

→ Base voltage must be negative w.r.t the emitter

→ Collector voltage must be negative w.r.t the base.

→ Collector voltage must be negative w.r.t the emitter.

Fig ⑲ shows voltage source connection to PNP transistor via resistors.

→ Base bias voltage V_{BB} is connected via resistor R_B & the collector supply V_{CC} is connected via resistor R_C.

→ The positive terminals of V_{BB} & V_{CC} are connected at the transistor emitter terminal.

→ To ensure reverse biasing of collector-base junction, V_{CC} must be much larger than V_{BB}.

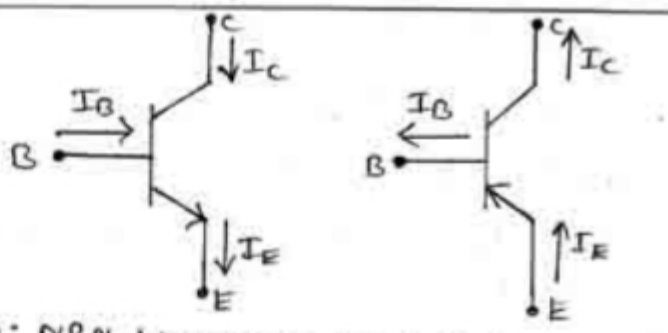
⑦ BJT currents:

Fig ⑳ shows npn & pnp transistor with currents.

Applying KCL to the transistor (as if it is a single node),

$$I_E = I_C + I_B$$

Note: The ratio of the transistor output current to the input current is called current gain of a transistor



(a): NPN transistor (b): PNP transistor

Fig (20): currents in transistor

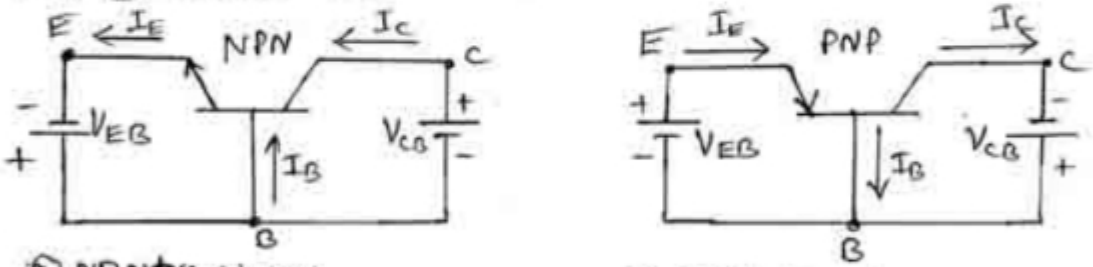
* **Transistor Configurations & Connections:**

There are three configurations of transistor.

1. Common base Connection
2. Common emitter connection.
3. Common Collector Connection.

1. Common base configuration:

Fig (21) shows the common base transistor circuit.



(a) NPN transistor (b) PNP transistor

Fig (21): Common base transistor.

→ Input is applied between the emitter & base terminals.

→ The output is taken between the collector & base terminals.

→ The emitter current is the input current & Collector current is the output current.

→ Input and output current may be either direct

current (or) alternating current.

④ Common base dc current gain (or) Current amplification factor (or) Small signal current gain (or) Common base, short circuit, amplification factor (or) Common base, short circuit current gain (α_{dc})

It is defined as the ratio of collector current (I_C) to the emitter current (I_E). It is denoted by α (or) α_{dc} (or) h_{FB}

ie $$\boxed{\alpha_{dc} = \frac{I_C}{I_E}}$$

⑤ Common base ac current gain (α_{ac})

It is defined as the ratio of small change in collector current (ΔI_C) to the small change in emitter current (ΔI_E) for a constant collector-to-base voltage (V_{CB})

(or)

It is defined as the ratio of change in collector current to the change in emitter current at constant collector-base voltage (V_{CB})

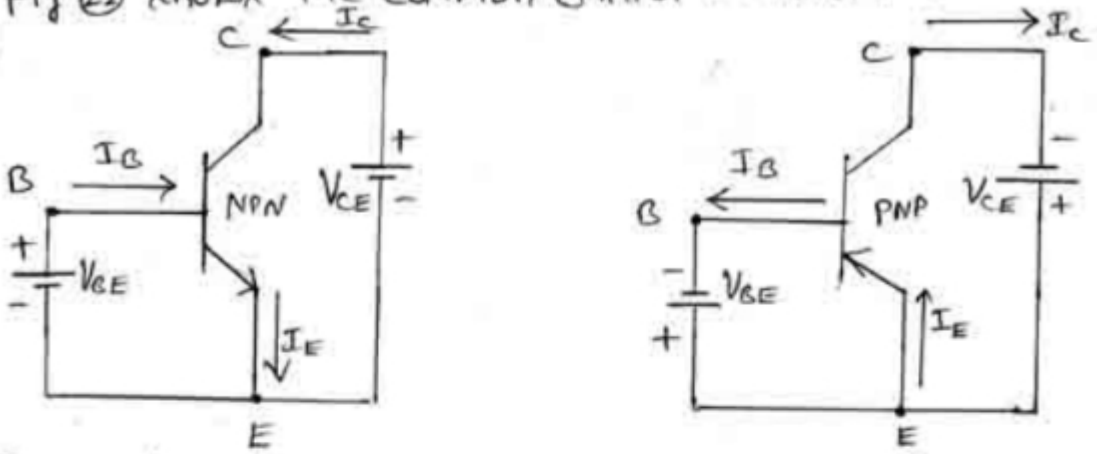
It is designated by α_0 (or) α_{ac} (or) h_{fb}

i.e $$\boxed{\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E}}$$ (or) $$\boxed{\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E}\Big|_{V_{CB}=\text{constant}}}$$

- In practice, $\alpha_{dc} = \alpha_{ac}$
- α_{dc} is typically from 0.90 to 0.998

② Common Emitter Connection:

Fig (22) shows the common emitter transistor circuit.



(a) NPN transistor (b) PNP transistor

Fig (22): Common emitter transistor

→ The base current is the input current & the collector current is the output current.

(a) Common emitter dc current gain (or) Large signal common-emitter current gain (or) Base current amplification factor (or) Common-emitter short circuit current gain (or) current gain from base to collector: (β_{dc})

It is defined as the ratio of collector current (I_C) to the base current (I_B). It is denoted by β (or) β_{dc} (or) h_{FE}.

ie $$\beta_{dc} = \frac{I_C}{I_B}$$

(b) Common emitter ac current gain (β_{ac})

It is defined as the ratio of change in collector (ΔI_C) current to the change in base current (ΔI_B) for a constant collector-to-emitter voltage (V_{CE}).

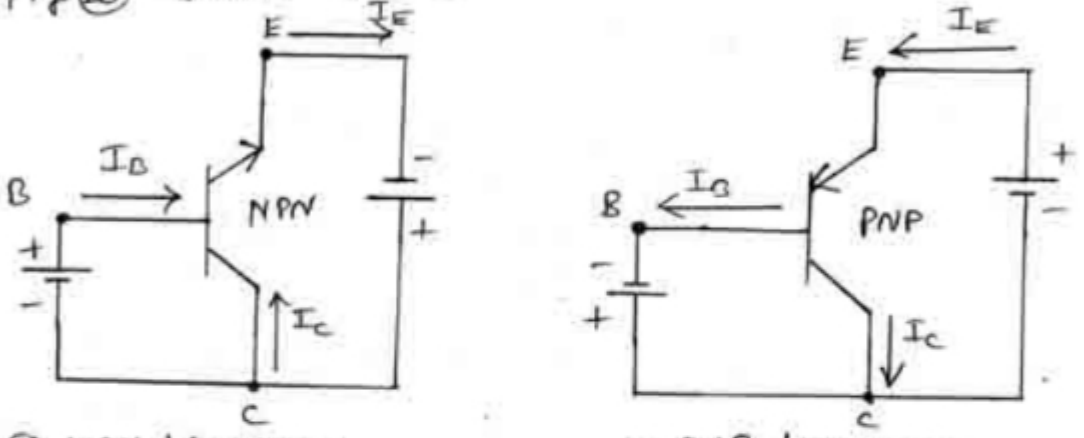
It is denoted by β_o (or) β_{ac} (or) h_{fe}

i.e $\boxed{\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}}$ (or) $\boxed{\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}\Big|_{V_{CE} = \text{constant}}}$

- In practice, $\beta_{ac} = \beta_{dc}$
- β_{dc} is typically from 20 to 500

③ Common collector configuration:

Fig (23) shows the common collector transistor circuit



ⓐ NPN transistor ⓑ PNP transistor

Fig (23): Common collector transistor

→ The base current is the input current & emitter current is the output current.

ⓐ Common-collector dc current gain (γ_{dc})

It is defined as the ratio of emitter current (I_E) to the base current (I_B). It is denoted by γ (or) γ_{dc} (or) h_{FC}

i.e $\boxed{\gamma_{dc} = \frac{I_E}{I_B}}$

ⓑ Common-collector ac current gain (γ_{ac})

It is defined as the ratio of change in emitter current (ΔI_E) to the change in base current (ΔI_B)

for a constant Emitter-to-collector voltage (V_{EC})

It is denoted by γ_0 (or) γ_{ac} (or) h_{fc}

i.e $\boxed{\gamma_{ac} = \frac{\Delta I_E}{\Delta I_B}}$ (or) $\boxed{\gamma_{ac} = \left.\frac{\Delta I_E}{\Delta I_B}\right|_{V_{EC} = \text{constant}}}$

- In Practice, $\gamma_{ac} = \gamma_{dc}$
- γ_{dc} is typically from 21 to 501.

* Relation between α_{dc} & β_{dc}

We know that

$$I_E = I_c + I_B \quad -(1)$$

Dividing (1) by I_c, we get

$$\frac{I_E}{I_c} = 1 + \frac{I_B}{I_c} \quad -(2)$$

We have $\alpha_{dc} = \frac{I_c}{I_E}$ & $\beta_{dc} = \frac{I_c}{I_B}$ —(*)

$$\Rightarrow \frac{1}{\alpha_{dc}} = \frac{I_E}{I_c} \quad -(3) \qquad \Rightarrow \frac{1}{\beta_{dc}} = \frac{I_B}{I_c} \quad -(4)$$

Using (3) & (4) in (2), we get

$$\frac{1}{\alpha_{dc}} = 1 + \frac{1}{\beta_{dc}} \quad -(5)$$

$$\Rightarrow \frac{1}{\alpha_{dc}} = \frac{\beta_{dc}+1}{\beta_{dc}}$$

$$\Rightarrow \boxed{\alpha_{dc} = \frac{\beta_{dc}}{\beta_{dc}+1}} \quad -(6)$$

Now eqn (5), we can write.

$$\frac{1}{\beta_{dc}} = \frac{1}{\alpha_{dc}} - 1$$

$$\frac{1}{\beta_{dc}} = \frac{1-\alpha_{dc}}{\alpha_{dc}}$$

$$\Rightarrow \boxed{\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}} \quad -(7)$$

* **Relation between β_{dc} & γ_{dc}:**

Consider eqn (1)

$$I_E = I_C + I_B$$

$\div$ by I_B

$$\frac{I_E}{I_B} = \frac{I_C}{I_B} + 1 \quad -(8)$$

We have, $\gamma_{dc} = \frac{I_E}{I_B}$ $-(9)$

Using (*) & (9) in (8), we get

$$\boxed{\gamma_{dc} = \beta_{dc} + 1} \quad -(10) \Rightarrow \boxed{\beta_{dc} = \gamma_{dc} - 1} \quad -(11)$$

* **Relation between α_{dc} & γ_{dc}:**

Using (7) in (10), we get

$$\gamma_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}} + 1$$

$$\Rightarrow \gamma_{dc} = \frac{\alpha_{dc} + 1 - \alpha_{dc}}{1-\alpha_{dc}}$$

$$\boxed{\gamma_{dc} = \frac{1}{1-\alpha_{dc}}} \quad -(12)$$

$$\Rightarrow 1 - \alpha_{dc} = \frac{1}{\gamma_{dc}}$$

$$\Rightarrow 1 - \frac{1}{\gamma_{dc}} = \alpha_{dc}$$

$$\Rightarrow \boxed{\alpha_{dc} = \frac{\gamma_{dc} - 1}{\gamma_{dc}}} \quad -(13)$$

* **Relation among α_{dc}, β_{dc} & γ_{dc}:**

We know that $\gamma_{dc} = \frac{I_E}{I_B}$

$\Rightarrow \gamma_{dc} = \frac{I_E/I_C}{I_B/I_C}$

$\Rightarrow \gamma_{dc} = \frac{1/\alpha_{dc}}{1/\beta_{dc}}$

$\Rightarrow \boxed{\gamma_{dc} = \frac{\beta_{dc}}{\alpha_{dc}}}$ — (14)

Note:

(1) I_C interms of I_B & α_{dc}

We have $\alpha_{dc} = \frac{I_C}{I_E}$

$\Rightarrow I_C = \alpha_{dc} I_E$

$\Rightarrow I_C = \alpha_{dc}(I_C + I_B)$ $(\because I_E = I_C + I_B)$

$\Rightarrow I_C(1-\alpha_{dc}) = \alpha_{dc} I_B$

$$\boxed{I_C = \frac{\alpha_{dc}}{1-\alpha_{dc}} I_B}$$ — (15)

(or)

We know $\beta_{dc} = \frac{I_C}{I_B}$

$\Rightarrow I_C = \beta_{dc} I_B$

$$\boxed{I_C = \frac{\alpha_{dc}}{1-\alpha_{dc}} I_B} \quad \left(\because \beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}\right)$$

(2) npn transistor → not pointing in

pnp transistor → pointing in

③ β_{dc} is defined by a simple ratio of dc currents at an operating point. Whereas the β_{ac} is sensitive to the characteristics in the region of interest.

④ Expression for collector current:

Consider a PNP transistor circuit as shown in fig (24)

ⓐ When switch is closed:

The forward bias voltage V_{EB} injects holes in the base region. The reverse bias voltage V_{CB} on the collector-base junction attracts the majority of holes from the base region & constitute collector current (injected current)

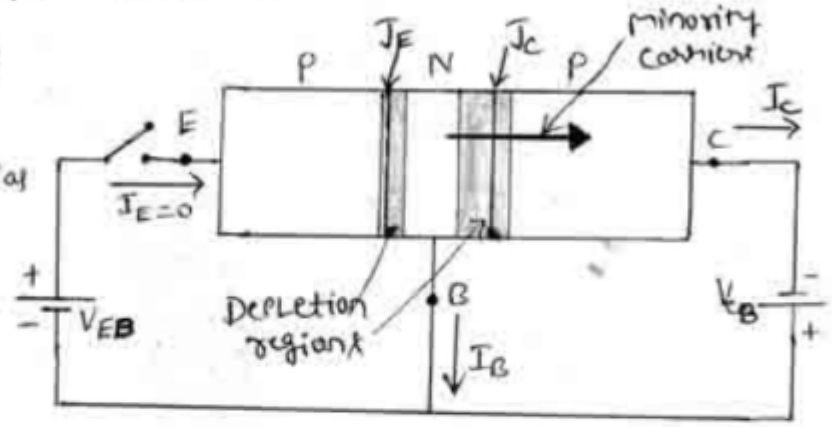


Fig (24): Common base PNP transistor

ie $I_C = \alpha_{dc} I_E$ (Due to majority carriers) (mA) —(16)

ⓑ When switch is open:

There is no emitter current & therefore no base current & no collector current. The minority carriers diffuse across the collector base junction & hence produce a current known as leakage current (I_{CBO}) ⓐ reverse saturation current ⓑ collector cut-off current ⓒ I_C current with emitter terminals open (I_{CO})

ie $I_C = I_{CBO}$. (Due to minority carrier ⓐ thermally generated carriers) (μA ⓑ nA) —(17)

The total collector current

$$I_C = \alpha_{dc} I_E + I_{CBO} \quad —(18)$$

$$\Rightarrow I_C = \alpha_{dc}(I_C + I_B) + I_{CBO} \quad (\because I_E = I_C + I_B)$$

$$\Rightarrow I_C - \alpha_{dc} I_C = \alpha_{dc} I_B + I_{CBO}$$

$$\Rightarrow I_C(1-\alpha_{dc}) = \alpha_{dc} I_B + I_{CBO}$$

$$\Rightarrow I_C = \frac{\alpha_{dc}}{1-\alpha_{dc}} I_B + \frac{1}{1-\alpha_{dc}} I_{CBO}$$

$$\boxed{I_C = \beta_{dc} I_B + (1+\beta_{dc}) I_{CBO}} \quad \text{— (19)}$$

Ltt

(1) $\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}$

Ltt

(2) $\frac{1}{1-\alpha_{dc}} = \frac{1}{1-\frac{\beta_{dc}}{1+\beta_{dc}}}$

$$\Rightarrow = \frac{1}{\frac{1+\beta_{dc}-\beta_{dc}}{1+\beta_{dc}}}$$

$$\frac{1}{1-\alpha_{dc}} = 1+\beta_{dc} \quad \text{— (20)}$$

(5) At room temperature

For Si transistor, $I_{CBO} \approx I_{CO} \rightarrow$ nA (can be neglected)

For Ge transistor, $I_{CBO} \approx I_{CO} \rightarrow$ mA (cannot be neglected)

(6) The value of I_{CBO} is strongly temperature dependent for both Si & Ge. It doubles for every 10°C increase in temperature.

(7) Si transistors can be used upto 200°C

Ge transistors can be used upto 100°C

(8) For common emitter configuration, (Common collector)

$$I_C = \beta_{dc} I_B + (1+\beta_{dc}) I_{CBO}$$

$$\Rightarrow \boxed{I_C = \beta_{dc} I_B + I_{CEO}} \quad \text{— (21)}$$

Where, I_{CEO} → Collector-Emitter current with base Open

$$= (1+\beta_{dc}) I_{CBO} \approx \frac{1}{1-\alpha_{dc}} I_{CBO} \Big|_{I_B=0\,mA}$$

Emitter current,

$$I_E = I_C + I_B$$

Using (21) we get

$$I_E = \beta_{dc} I_B + I_{CEO} + I_B$$

$$\boxed{I_E = (1+\beta_{dc}) I_B + I_{CEO}} \quad \text{— (22)}$$

* BJT amplification (or) Transistor as an amplifier :

(1) Current amplification (or) Transistor as a current amplifier :

→ The current amplifier (NPN transistor) is shown in fig (25).

→ A small change (Increase (or) decrease) in base current (ΔI_B) produces a large change (Increase (or) decrease) in collector current (ΔI_C) & a large emitter current change (Increase (or) decrease) (ΔI_E) [Shown in fig (26) (a) & (b)]

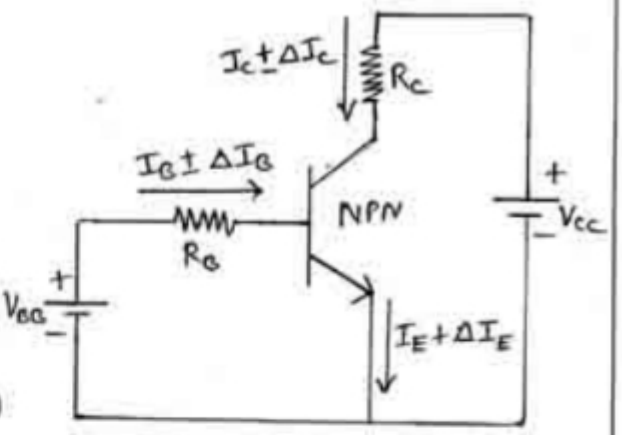


Fig (25) : Current amplifier

→ The common emitter current gain is the ratio of change in collector current (ΔI_C) (output current) to the change in base current (ΔI_B) (input current). It is denoted by β_{ac} (or) h_{fe}

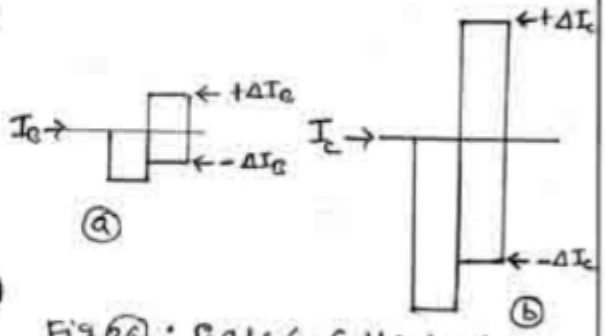


Fig (26) : Base & Collector Currents

i.e $\beta_{ac} = \dfrac{\Delta I_C}{\Delta I_B}$

Where, $\Delta I_C \rightarrow$ AC collector current, denoted by I_c

$\Delta I_B \rightarrow$ AC base current, denoted by I_b

$\therefore \boxed{\beta_{ac} = \dfrac{I_c}{I_b}}$

Ex: If $I_b = \pm 1\,mA$ (Assume $\beta = 100$), then

$I_c = \beta_{ac} I_b = 100 \times \pm 1\,mA = \pm 0.1\,mA$

∴ A small change in the base current, produces a large change in collector current.

Hence transistor acts as current amplifier.

② Voltage amplification ⓐ Transistor as a voltage amplifier:

→ The voltage amplifier (NPN transistor) is shown in fig (27).

→ The dc voltage $V_{BB} = 0.7V$ forward biases the base-emitter junction.

→ An AC voltage source (V_i) in series with V_{BB} provides a $\pm 20mV$ input voltage variation.

→ Let the transistor is connected to a $V_{cc} = 20V$ dc voltage source via $R_c = 12K\Omega$ resistor & let $\beta_{dc} = 50$

→ The V_{BE} Vs I_B characteristics is shown in fig (28)

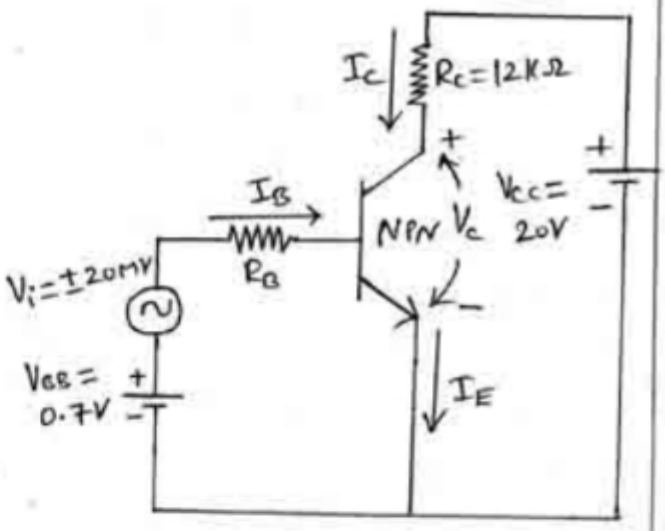


Fig (27): Voltage amplifier

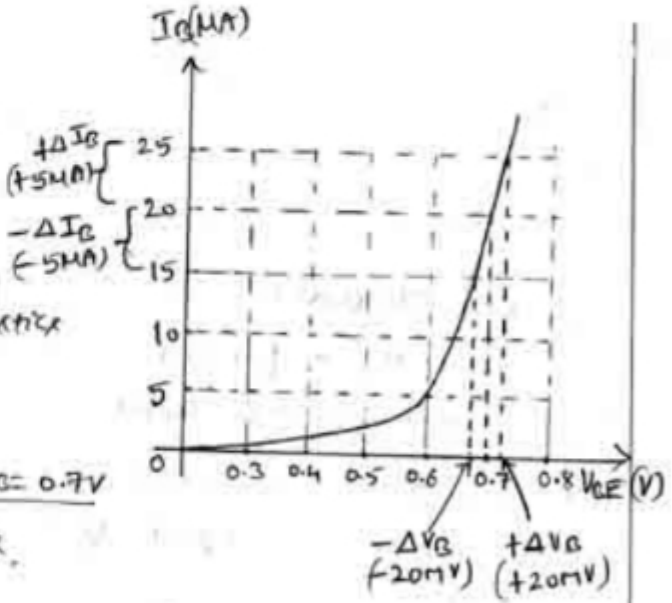


Fig (28): V_{BE} Vs I_B Characteristics

→ Case (i): When $V_i = 0V$, $V_{BB} = 0.7V$

From the characteristics,

$I_B = 20\mu A$

Collector current,

$$I_c = \beta_{dc} I_B = 50 \times 20 \times 10^{-6} = 1mA$$

Collector voltage (Applying KVL to loop containing V_{cc}, R_c & V_c)

$$V_c = V_{cc} - I_c R_c = 20V - 1 \times 10^{-3} \times 12 \times 10^{3} = 8V$$

- Case (ii): When $V_i = \pm 20mV$

From the characteristics, Change in base current,

$$\Delta I_B = \pm 5\mu A$$

Change (Variation) in collector current,

$$\Delta I_c = \beta_{dc} I_B = 50 (\pm 5\,\mu A) = \pm 250\,\mu A$$

Change (Variation) in collector voltage,

$$\Delta V_c = \Delta I_c \times R_c = \pm 250\,\mu A \times 12\,k\Omega = \pm 3V$$

→ Since the output voltage ($\Delta V_c = \pm 3V$) is greater than the input voltage ($\Delta V_B = \pm 20mV$), the transistor circuit is voltage amplifier.

→ Voltage gain (A_V) is the ratio of the output voltage to the input voltage.

$$\text{ie } A_V = \frac{\Delta V_c}{\Delta V_B} = \frac{\pm 3V}{\pm 20mV} = 150$$

* Transistor characteristics ⓐ Characteristics of transistor

The important characteristics of transistor are

ⓐ Input characteristics ⓑ output characteristics

ⓒ current gain characteristics.

ⓐ Input characteristics : It is a plot of input current as a function of input voltage, keeping the output voltage constant.

ⓑ output characteristics : It is a plot of output current Vs output voltage at constant input current.

ⓒ current gain characteristics ⓓ Forward transfer characteristics : It is a plot of output current Vs input current at constant output voltage.

① Common base configuration :

Fig (29) shows common base PNP transistor.

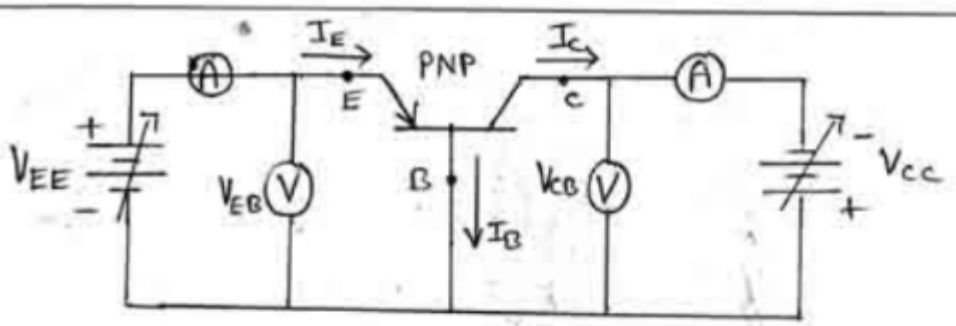


Fig (29): Common base PNP transistor

→ Input Characteristics: (Fig 30)

- It is a plot of input current (I_E) Vs input voltage (V_{EB}) at constant output voltage (V_{CB}).

- Procedure:

① Keeping V_{CB} constant at particular value, increase V_{EB} in small suitable steps & note down the corresponding values of I_E.

② The above step is repeated for different output voltage (V_{CB}) values

③ A graph of I_E along Y-axis & V_{EB} along X-axis for each value of V_{CB} is plotted.

- observations:

① Below threshold voltage or offset voltage or cut-in voltage or knee voltage 'V_γ', I_E is negligibly small ($V_\gamma \simeq 0.3V$ for Ge & $0.7V$ for Si)

② Beyond V_γ, for a fixed V_{CB} voltage, the I_E increases rapidly with a small increase in V_{EB}

③ As V_{CB} is increased, the curves shift upwards.

④ AC input resistance,

$$R_i = \frac{\Delta V_{EB}}{\Delta I_E} \Big|_{V_{CB}=\text{constant}}$$ (It is very low, typically 50Ω)

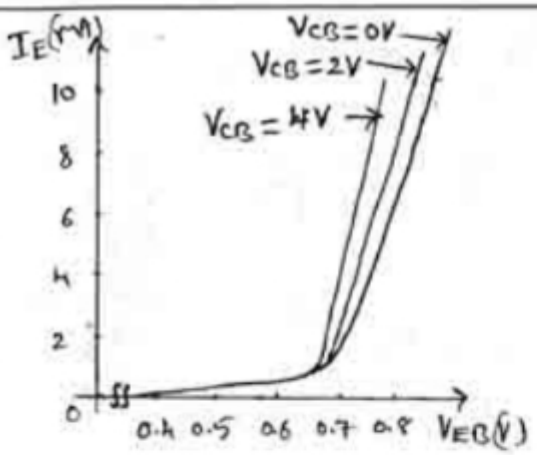


Fig (30): Input characteristics

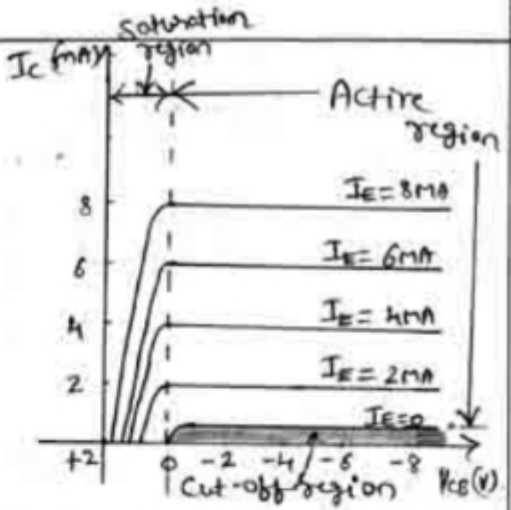


Fig (31): output characteristics

→ Output characteristics (Fig 31)

- It is a plot of output current (I_C) Vs output voltage (V_{CB}) at constant input current (I_E).
- Procedure:

① Keeping I_E constant at particular value, increase V_{CB} in suitable steps & note down (record) the corresponding values of I_C

② The above step is repeated for different input current values (I_E)

③ A graph of V_{CB} along X-axis & I_C along Y-axis for each value of I_E is plotted.

- Observations:

① The output characteristics has three important regions namely Saturation region, active region & cut-off region.

Saturation region

ⓐ It is the region to the left of the vertical dashed line

ⓑ In this region, both emitter-base & collector-base

junctions are forward biased

(c) In this region, a small change in V_{CB} results in a large value of current I_C.

Active region

(a) It is the region between the vertical dashed line & the horizontal axis.

(b) In this region, emitter-base junction is forward biased & collector-base junction is reverse biased.

(c) In this region, the collector current is constant and is equal to the emitter current.

Cut-off region

(a) It is the region along the horizontal axis as shown by a shaded region.

(b) In this region, both emitter-base & collector-base junctions are reverse biased.

(c) It corresponds to the curve marked $I_E = 0$

(2) I_C flows even when the V_{CB} is zero.

(3) A small collector current (Leakage current 'I_{CBO}') flows even when $I_E = 0$

(4) I_C is practically independent of V_{CB} in the active region. However, if V_{CB} is increased beyond a certain large value, the collector current increases rapidly due to avalanche breakdown (not shown in fig) & the transistor action is lost.

(5) Ac output resistance.

$$R_o = \frac{\Delta V_{CB}}{\Delta I_C}\Big|_{I_E = \text{Constant}}$$ (It is very high & typically about 500 kΩ)

→ Current gain characteristics (Forward transfer characteristics) (Fig 32)

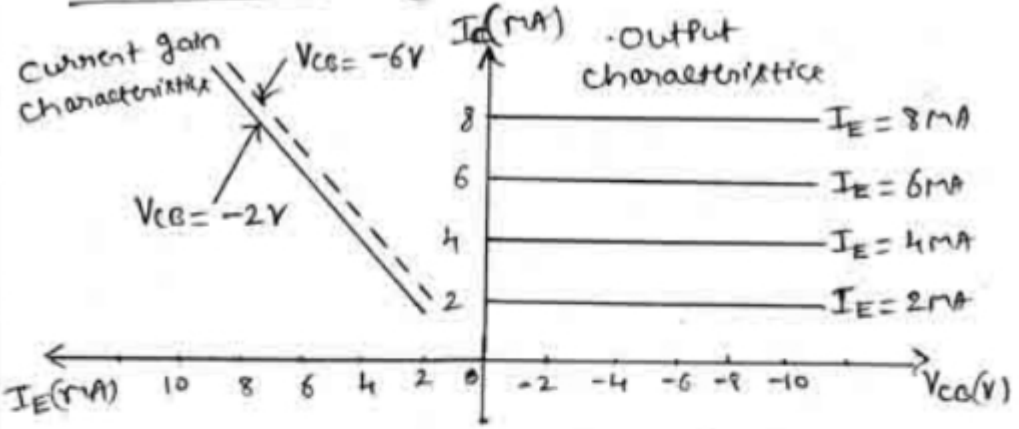


Fig (32): Current gain characteristics

- It is a plot of output current (I_C) versus input current (I_E) at constant output voltage (V_{CB})
- Procedure:

① Keeping V_{CB} constant at particular value, I_C is measured for various levels of I_E

② A graph of I_C vs I_E is plotted.

3) Common Emitter Configuration:

Fig (33) Shows Common Emitter PNP transistor.

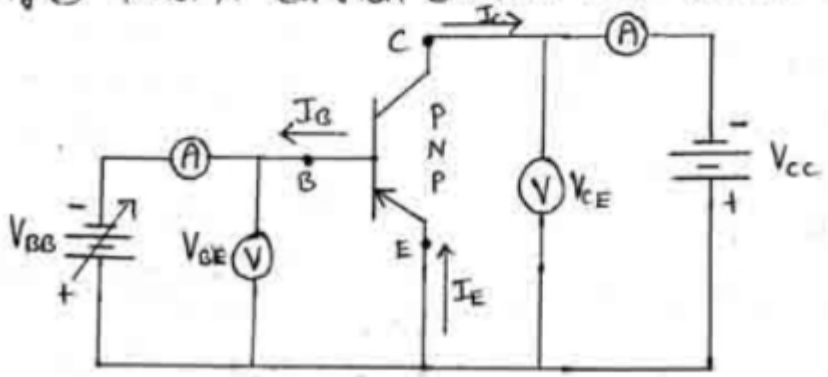


Fig (33): Common Emitter PNP transistor

→ Input Characteristics: (Fig 34)

- It is a plot of input current (I_B) vs input voltage (V_{BE}) at constant output voltage (V_{CE}).

- Procedure:

① Keeping V_{CE} constant at particular value, increase V_{BE} in small suitable steps & noted down the corresponding values of I_B.

② The above step is repeated for different output voltage (V_{CE}) values.

③ A graph of I_B along Y-axis & V_{BE} along X-axis for each value of V_{CE} is plotted.

- Observations:

① Below threshold voltage @ Knee voltage 'V_γ', I_B is negligibly small.

② Beyond V_γ, for a fixed V_{CE} voltage, the I_B increases rapidly with a small increase in V_{BE}.

③ As V_{CE} is increased, the curves shift downwards.

④ AC input resistance.

$$R_i = \frac{\Delta V_{BE}}{\Delta I_B} \Big|_{V_{CE} = \text{Constant}}$$

(It is low & typically ranges from 600Ω to 4000Ω)

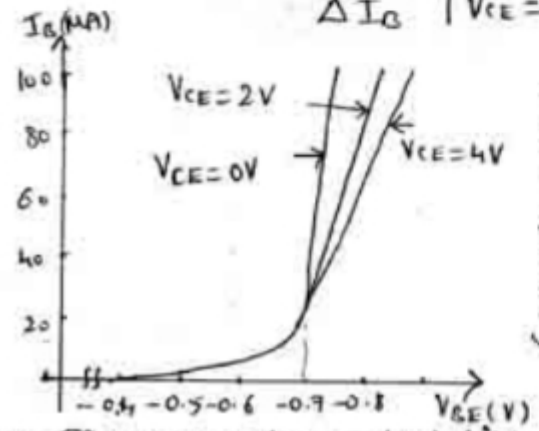


Fig (34): Input characteristics

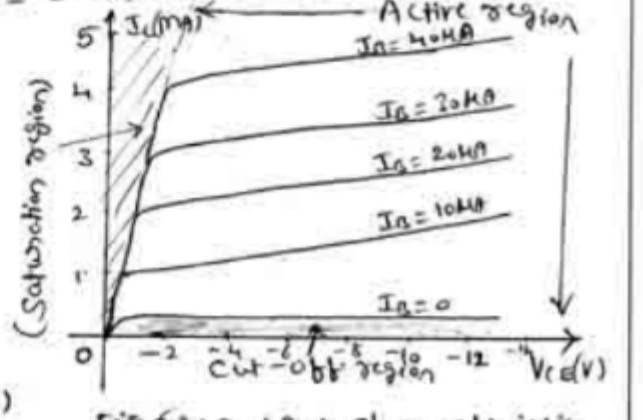


Fig (35): Output characteristics

→ Output characteristics (Fig 35)

- It is a plot of output current (I_C) Vs output voltage (V_{CE}) at constant input current (I_B).

- Procedure:

① Keeping I_B constant at particular value, increase (V_{CE}) in suitable steps & note down the corresponding values of I_C.

② The above step is repeated for different input current values (I_B).

③ A graph of V_{CE} along X-axis & I_C along Y-axis for each value of I_B is plotted.

- Observations:

① The output characteristics has three important regions namely saturation region, active region & cut-off region

Saturation region:

ⓐ It is the region shown by the shaded area

ⓑ In this region, both base-emitter & collector-emitter junctions are forward biased.

ⓒ In this region, a small change in V_{CE} results in a large value of current 'I_C'.

Active region

ⓐ It is the region between the saturation & cut-off region.

ⓑ In this region, base-emitter junction is forward biased & collector-emitter junction is reverse biased.

ⓒ In this region, when V_{CE} is increased further, I_C increases slightly.

Cut-off region

① It is the region along the horizontal axis as shown by a shaded region (corresponds to curve marked $I_B=0$)

② In this region, both base-emitter & collector-emitter junctions are reverse biased.

③ I_C increases rapidly to a saturation value, when V_{CE} is increased above zero (depending upon the value of I_B)

④ A small collector current (Leakage current I_{CEO}) flows even when $I_B=0$.

⑤ If V_{CE} is increased beyond a certain value, the I_C increases rapidly due to avalanche breakdown (not shown in fig) & the transistor action is lost.

⑥ AC output resistance.

$$R_o = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_B=\text{Constant}}$$

(It is high & typically ranges from 10KΩ to 50KΩ)

→ Current gain ⑦ Forward transfer characteristics (Fig 36)

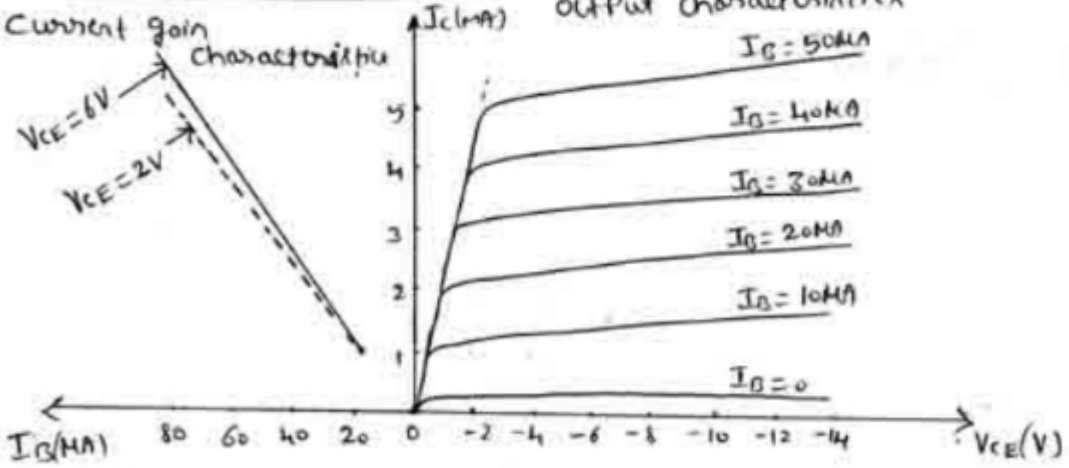


Fig ⑧: Current gain characteristics

- It is a plot of output current (I_C) versus input current (I_B) at constant output voltage (V_{CE}).

• Procedure

① Keeping V_{CE} constant at particular value. I_C is measured for various levels of I_B.

② A graph of I_C Vs I_B is plotted

• Current gain characteristics can be obtained experimentally (Fig 33) or derived from the output characteristics (Fig 36)

③ Common Collector Configuration:

Fig (37) Shows Common Collector PNP transistor

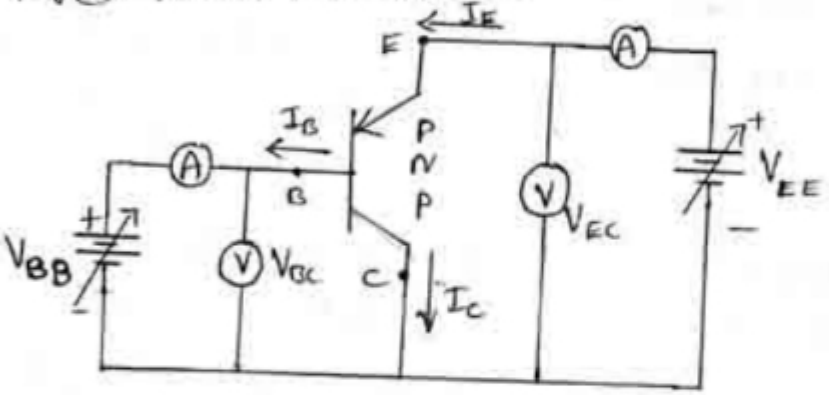


Fig (37): Common Collector PNP transistor

→ Input Characteristics (Fig 39)

• It is a Plot of input current (I_B) Vs input voltage (V_{BC}) at constant output voltage (V_{EC})

• Procedure:

① Keeping V_{EC} constant at particular value, increase V_{BC} in small suitable steps & note down the corresponding values of I_B.

② The above step is repeated for different output voltage values (V_{EC})

③ A graph of I_B along Y-axis & V_{BC} along X-axis

for each value of V_{EC} I_B is plotted.

- **Observations:**

① Applying KVL around the transistor, (Fig 37 or Fig 31)

$$V_{EC} - V_{EB} - V_{BC} = 0$$

$$\Rightarrow \boxed{V_{EB} = V_{EC} - V_{BC}}$$

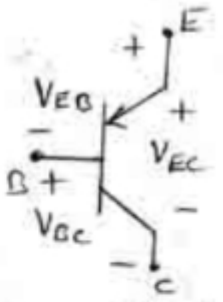


Fig 38: Common collector CKt

② Increasing V_{BC} with V_{EC} held constant reduces the V_{EB} & thus reduces I_B. This explains the slope of the CC input characteristics.

③ As V_{EC} is increased, the curves shift rightside.

④ AC input resistance

$$R_i = \left.\frac{\Delta V_{BC}}{\Delta I_B}\right|_{V_{EC}=\text{Constant}}$$

(It is very high & about 750KΩ)

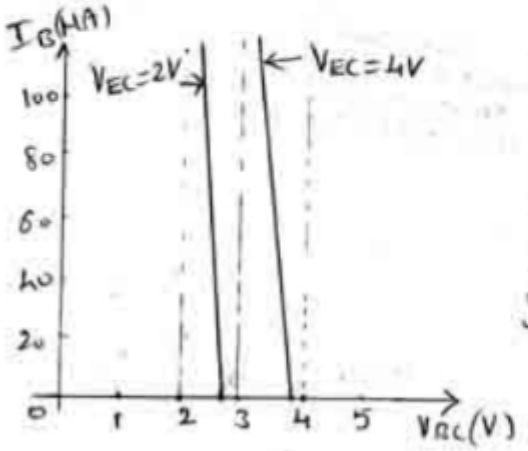


Fig 39: Input characteristics

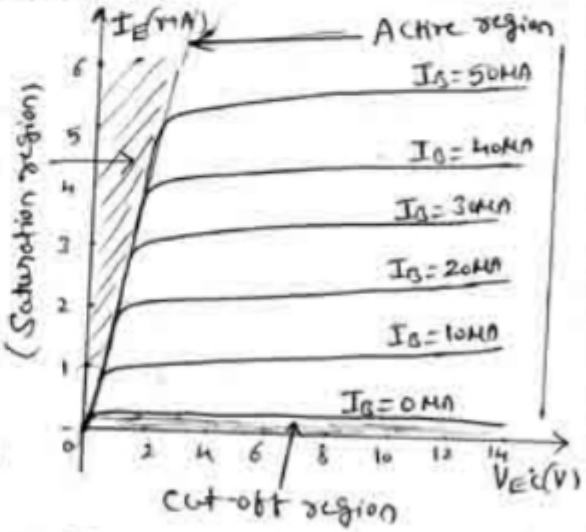


Fig 40: Output characteristics

→ **Output Characteristics (Fig 40)**

- It is a plot of output current (I_E) Vs output voltage (V_{EC}) at constant input current (I_B).

- Procedure:

① Keeping I_B constant at particular value, increase (V_{EC}) in suitable steps & noted down the corresponding values of I_E

② The above step is repeated for different input current values I_B.

③ A graph of V_{EC} along X-axis & I_E along Y-axis for each value of I_B is plotted.

- Observations:

① The output characteristics has three important regions namely saturation, active & cut-off region.

Saturation region

ⓐ It is the region shown by the shaded area.

ⓑ In this region, both base-collector & emitter-collector junctions are forward biased.

ⓒ In this region, a small change in V_{EC} results in a large value of current I_E.

Active region

ⓐ It is the region between the saturation & cut-off region.

ⓑ In this region, base-collector junction is forward biased & emitter-collector junction is reverse biased.

ⓒ In this region, when V_{EC} is increased further, I_E increases slightly

Cut-off region

ⓐ It is the region along the horizontal axis as shown by a shaded area (corresponds to curve marked $I_B = 0$).

⑥ In this region, both base-Collector & emitter-Collector junctions are reverse biased.

② I_E increases rapidly to a saturation value, when V_{EC} is increased above zero (depending upon the value of I_B)

③ A small collector current (Leakage current I_{CO}) flows even when $I_B = 0$.

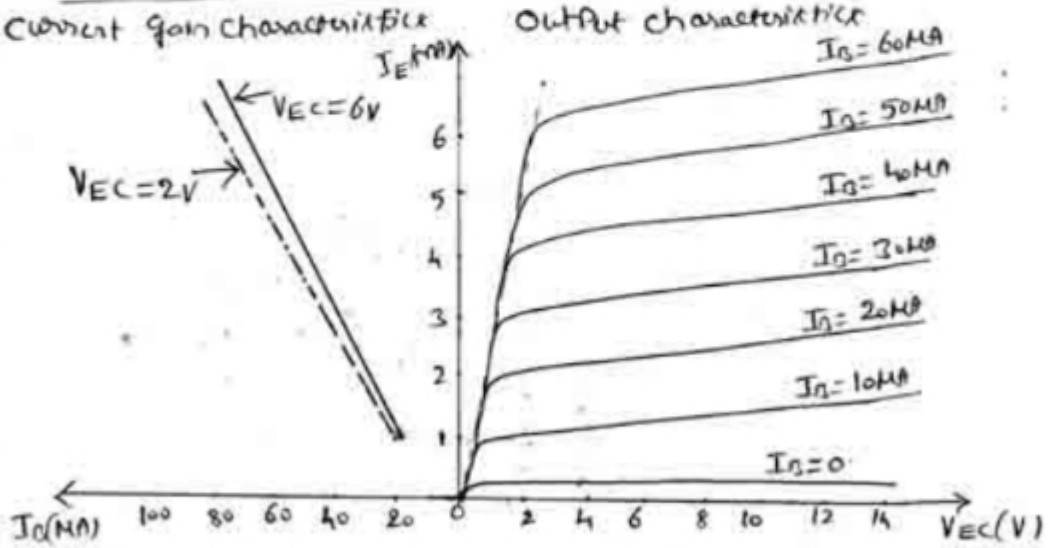
④ In V_{EC} is increased beyond a certain value, the I_C increases rapidly due to avalanche breakdown (not shown in fig) & the transistor action is lost.

⑤ AC output resistance

$$R_o = \left.\frac{\Delta V_{EC}}{\Delta I_E}\right|_{I_B = \text{constant}}$$

(It is very low & is about 50Ω)

→ Current gain @ Forward transfer characteristics (Fig 41)



Fig(41): current gain characteristics

- It is a plot of output current (I_E) versus input current (I_B) at constant output voltage (V_{EC})
- current gain characteristics can be obtained experimentally (Fig 37) or derived from the output characteristics (Fig 41)

• Procedure

① Keeping V_{EC} constant at particular value, I_E is measured for various levels of I_B.

② A graph of I_E vs I_B is plotted.

Note: ① In transistor, voltage breakdown occurs in two types namely

ⓐ Avalanche breakdown: It is a form of voltage breakdown that arises, when the electrons & holes in the semiconductor are accelerated enough by the applied voltage. The accelerated electrons & holes collide with the bound electrons and produce more free electrons. This causes even more collisions due to which current increases to a large value.

ⓑ Punch through @ reach-through: It is a form of voltage breakdown that arises due to the increased width of collector @ base junction depletion region with increased collector-base junction voltage (This phenomenon of reducing the base width is called early effect @ base-width modulation). The depletion region at a junction is the region of fixed ions on both sides of the junction. As the applied voltage across the junction increases, the depletion region penetrates deeper into the base. Since the base is very thin, therefore it is possible that at moderate voltages, the depletion region will have spread completely across the base to reach the emitter-base junction. As a result of this, the current increases to a very large value.

② Common emitter circuit is most efficient

Main reasons are

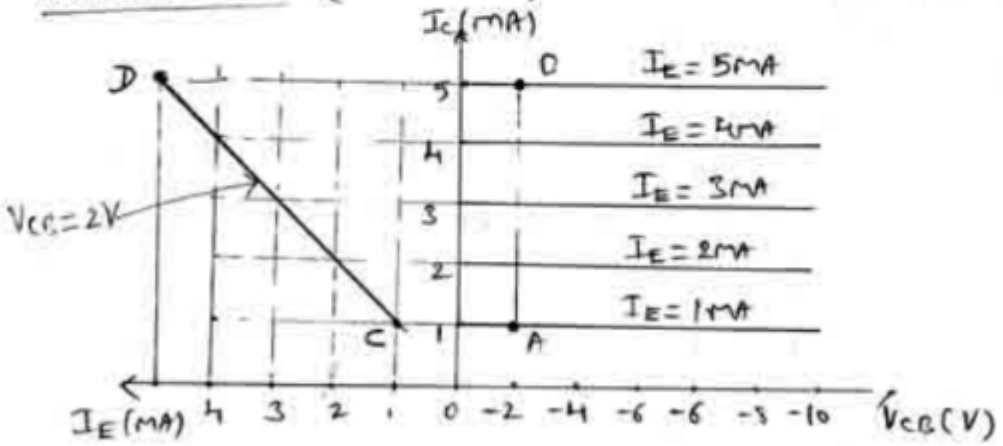
ⓐ High current gain: In CE connection, $I_C = \beta_{ac} I_B$ (or) $I_C = \beta_{dc} I_B + I_{CEO}$. As β_{dc} is very large, the output current I_C is much more than I_B.

∴ current gain in CE arrangement is very high (20 to 500)

ⓑ High voltage & power gain: Due to high current gain, CE ckt has the highest voltage & power gain.

ⓒ Moderate output to input impedance ratio: In CE ckt, the ratio of output impedance to input impedance is small (about 20). So it is ideal one for coupling between various transistor stages. [In CB & CC ckts this ratio is very large]

③ Driving current gain characteristics from output characteristics (Considering CB configuration)



Let $V_{CB} = -2V$

Step 1: Draw a vertical line through given V_{CB} value.

Step 2: Line intersects the characteristics at points A & B (Note down I_E & I_C) (Here $I_E \simeq I_C$)

Step 3: Plot points C & D for the output characteristics

at the corresponding levels of I_C & I_E.

Step 4: Draw the characteristic through points C & D.

(4) Advantages, Disadvantages & Applications of transistors

Advantages:

- They are mechanically strong
- Much smaller
- More compact
- Light weight
- Practically unlimited life (Last for many years)
- No heater requirement
- Transistors along with resistors and diodes can be integrated to produce ICs
- No heater loss
- Low operating voltages
- No warm-up period
- Less power observed by the device itself
- High voltage gain

Disadvantages:

- Drive circuit of BJT is complex
- Storage charge in base reduces switching frequencies
- Cannot be used in high power applications
- Lower input impedance
- Temperature dependence
- Inherent variation of parameters (β_{dc} for 148 transistors may vary between 100 & 600)

Applications:

- Switched mode power supplies (SMPS)
- DC to DC converters (Choppers)
- Bridge inverters
- Power factor correction techniques
- Amplifiers
- Switches
- Impedance matching

(5) Comparision of CB, CE & CC Configurations

Sl no.	Characteristic	CB	CE	CC
1)	Input resistance	Very low (50Ω)	Low (600Ω)	Very high (750kΩ)
2)	Output resistance	Very high (500kΩ)	High (10kΩ)	Low (50Ω)
3)	Current gain	Less than unity	Greater than unity	Greater than unity
4)	Voltage gain	Medium (about 150)	Medium (about 500)	Low (< 1)
5)	Input current	I_E	I_B	I_B
6)	Output current	I_C	I_C	I_E
7)	Input terminals	E & B	B & E	B & C
8)	Output terminals	C & B	C & E	E & C
9)	Current amplification factor	$\alpha_{dc} = \frac{I_C}{I_E}$	$\beta_{dc} = \frac{I_C}{I_B}$	$\gamma_{dc} = \frac{I_E}{I_B}$
10)	Phase between input & output	In-phase (0°)	Out-of-phase (180°)	In-phase (0°)
11)	Applications	For high frequency applications	For audio frequency application	For impedance matching

Problems

① In a common base connection, a certain transistor has an emitter current of 10mA & a collector current of 9.8mA. Calculate the value of the base current.

Sol: Given $I_E = 10mA$, $I_C = 9.8mA$, $I_B = ?$

We have, $I_E = I_C + I_B$

$\Rightarrow I_B = I_E - I_C$

$= 10 \times 10^{-3} - 9.8 \times 10^{-3}$

$\boxed{I_B = 0.2mA}$

② In a common-base connection, the emitter current is 6.28mA & the collector current is 6.20mA. Determine the common-base dc current gain.

Sol: Given $I_E = 6.28mA$, $I_C = 6.20mA$, $\alpha_{dc} = ?$

We have, $\alpha_{dc} = \frac{I_C}{I_E} = \frac{6.20 \times 10^{-3}}{6.28 \times 10^{-3}} = 0.987$

③ The common-base dc current gain of a transistor is 0.967. If the emitter current is 10mA, what is the value of base current?

Sol: Given $\alpha_{dc} = 0.967$, $I_E = 10mA$, $I_B = ?$

We have, $I_C = \alpha_{dc} I_E \quad \left(\because \alpha_{dc} = \frac{I_C}{I_E}\right)$

$= 0.967 \times 10 \times 10^{-3}$

$I_C = 9.67mA$

By KCL $I_E = I_C + I_B$

$\Rightarrow I_B = I_E - I_C = 10 \times 10^{-3} - 9.67 \times 10^{-3}$

$\therefore \boxed{I_B = 0.33mA}$

(4) (a) A transistor has an α of 0.975, what is the value of β (b) if $\beta = 200$, what is the value of α?

Sol:

(a) Given $\alpha = 0.975$, $\beta = ?$

We have, $\beta = \frac{\alpha}{1-\alpha}$

$= \frac{0.975}{1-0.975}$

$\boxed{\beta = 39}$ //.

(b) Given, $\beta = 200$, $\alpha = ?$

We have, $\alpha = \frac{\beta}{1+\beta}$

$= \frac{200}{200+1}$

$\boxed{\alpha = 0.995}$ //.

(5) A transistor has a typical β of 100. If the collector current is 40mA, what is the emitter current?

Sol: Given $\beta = 100$, $I_C = 40mA$, $I_E = ?$

We have $I_B = \frac{I_C}{\beta}$ $\left(\because \beta = \frac{I_C}{I_B}\right)$

$= \frac{40 \times 10^{-3}}{100}$

$\boxed{I_B = 0.4mA \text{ @ } 400\,\mu A}$ //.

Now, $I_E = I_C + I_C = 0.4 \times 10^{-3} + 40 \times 10^{-3} = 40.4mA$

(6) A transistor has $\beta = 150$. Calculate the approximate collector & base currents, if the emitter current is 10mA.

Sol:

Given, $\beta = 150$, $I_E = 10mA$, $I_B = ?$, $I_C = ?$

We have $\alpha = \frac{\beta}{1+\beta} = \frac{150}{1+150} = 0.993$

Also $\alpha = \frac{I_C}{I_E}$

$\Rightarrow I_C = \alpha I_E = 0.993 \times 10 \times 10^{-3} = 9.93mA$ //.

Now, $I_B = I_E - I_C = 10 \times 10^{-3} - 9.93 \times 10^{-3} = 0.07mA$ $(\because I_E = I_C + I_B)$

(7) Determine the value of I_C & I_B for ckt shown in fig (7)

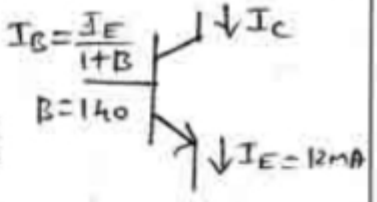


Fig (7)

Sol:

Given $I_E = 12mA$, $\beta = 140$. $I_B = \frac{I_E}{1+\beta}$

$\therefore I_B = \frac{12 \times 10^{-3}}{1+140} = 0.085\ mA$

Now $I_C = I_E - I_B = 12 - 0.085 \times 10^{-3} = 11.915mA$

(8) A transistor has $I_B = 105\mu A$ & $I_C = 2.05mA$. Find (a) β (b) α (c) I_E (d) If I_B changes by $27\mu A$ & I_C changes by $0.65mA$, find the new value of β.

Sol: Given $I_B = 105\mu A$, $I_C = 2.05mA$. (a) $\beta = ?$ (b) $\alpha = ?$, (c) $I_E = ?$

(d) $I_B' = I_B + 27\mu A$, $I_C' = I_C + 0.65mA$, $\beta' = ?$

(a) $\beta = \frac{I_C}{I_B} = \frac{2.05 \times 10^{-3}}{105 \times 10^{-6}} = 19.5$

(b) $\alpha = \frac{\beta}{1+\beta} = \frac{19.5}{1+19.5} = 0.95$

(c) $I_E = I_B + I_C = 105 \times 10^{-6} + 2.05 \times 10^{-3} = 2.155mA$

(d) $I_B' = I_B + 27\mu A = 105 \times 10^{-6} + 27 \times 10^{-6} = 132 \times 10^{-6} A$

$I_C' = I_C + 0.65mA = 2.05 \times 10^{-3} + 0.65 \times 10^{-3} = 2.7 \times 10^{-3} A$

New value of β, $\beta' = \frac{I_C'}{I_B'} = \frac{2.7 \times 10^{-3}}{132 \times 10^{-6}} = 20.5$

(9) A custom transistor has $\alpha = 0.98$, $I_{CO} = 5\mu A$ & $I_B = 100\mu A$. Find the values of Collector & Emitter Currents

Sol: Given $\alpha = 0.98$, $I_{CO} = 5\,\mu A$, $I_B = 100\,\mu A$, $I_C = ?$ $I_E = ?$

We get $I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CO}}{1-\alpha}$

$= \frac{0.98}{1-0.98} 100\times10^{-6} + \frac{5\times10^{-6}}{1-0.98}$

$\boxed{I_C = 5.15\,mA}$ //

We have $I_E = I_B + I_C = 100\times10^{-6} + 5.15\times10^{-3} = 5.25\,mA$

(10) A transistor has a maximum power dissipation of 500mW at 25°C. The derating factor is 2.28 mW/°C. What is the maximum power dissipation at 70°C?

Sol: Given $P_{D(max)} = 500\times10^{-3}$ W at 25°C

$DF = 2.28\,mW/°C$.

$P_{D(max)} = ?$, at $T = 70°C$

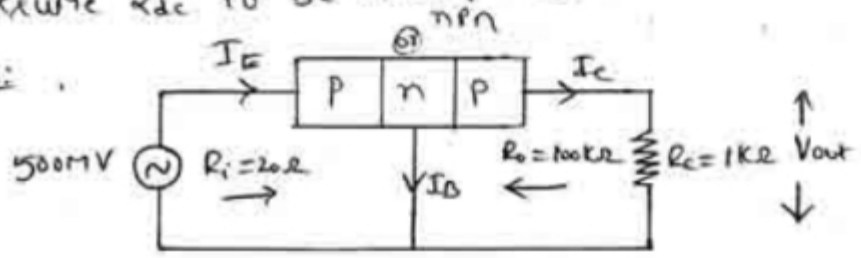
We have. $P_{D(max)(70°)} = P_{D(max)} - DF(T-25)$

$= 500\times10^{-3} - 2.28\times10^{-3}(70-25)$

$= 0.397$ W

(11) A common base transistor amplifier has an input resistance of 20Ω & output resistance of 100 KΩ. The collector load is 1KΩ if a signal of 500mV is applied between emitter and base, find the voltage amplification. Assume α_{dc} to be nearly one.

Sol:



Input Current $I_E = \frac{\text{Input Voltage}}{\text{Input resistance}}$

$= \frac{500 \times 10^{-3}}{20}$

$I_E = 25\text{mA}$

Now, $I_C = I_E$

$I_C = 25\text{mA}$

[$\because \alpha_{dc} = \frac{I_C}{I_E}$

$1 = \frac{I_C}{I_E}$ $\because \alpha_{dc} \simeq 1$ given

$I_E = I_C$]

Output voltage,

$V_{out} = I_C R_C$

$= 25 \times 10^{-3} \times 1 \times 10^{3}$

$= 25\text{V}$ //.

Voltage amplification (Voltage gain) is,

$A_V = \frac{V_{out}}{i/p\ V\text{tg}} = \frac{25}{500 \times 10^{-3}} = 50$ //.

(12) In a common base connection, the emitter current is 1mA. If the emitter circuit is open, the collector current is 50μA. Find the total collector current

Given $\alpha = 0.92$

Sol: Given, $I_E = 1\text{mA}$, $I_{CBO} = 50\mu\text{A}$, $I_C = ?$, $\alpha = 0.92$

We have, $I_C = \alpha I_E + I_{CBO} = 0.92 \times 1 \times 10^{-3} + 50 \times 10^{-6}$

$\boxed{I_C = 0.97\text{mA}}$ //.

(13) In a common base connection, $\alpha = 0.95$. The voltage drop across 2kΩ resistance which is connected in the collector is 2V. Find the base current.

Sol: Fig (13) shows common base ckt.

Given, $\alpha = 0.95$, $R_C = 2\text{k}\Omega$, $V_C = 2\text{V}$, $I_B = ?$

We have, $I_c = \frac{V_c}{R_c} = \frac{2V}{2k\Omega} = 1mA$

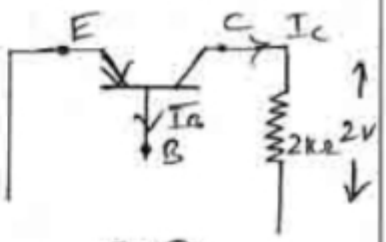


Fig (13)

We have, $I_E = \frac{I_c}{\alpha}$ $\left(\because \alpha = \frac{I_c}{I_E}\right)$

$= \frac{1\times10^{-3}}{0.95}$

$= 1.05mA$

Now $I_B = I_E - I_c = 1.05\times10^{-3} - 1\times10^{-2} = 0.05mA$

(4) For the common base CKt shown in fig (14), determine I_c & V_{CB}. Assume Si transistor.

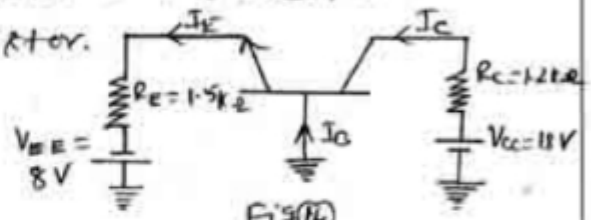


Fig (14)

Sol: Given, $R_E = 1.5k\Omega$, $V_{EE} = 8V$, $R_c = 1.2k\Omega$, $V_{cc} = 18V$,

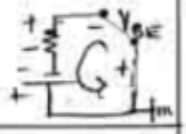
$V_{BE} = 0.7V$ (given Si transistor)

Applying KVL to emitter side loop,

$V_{EE} = I_E R_E + V_{BE}$

$\Rightarrow I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{8 - 0.7}{1.5\times10^{3}} = 4.87mA$

Actually $I_E = \frac{-V_{BE} - (-V_{EE})}{R_E}$



Let $I_c \simeq I_E \simeq 4.87mA$ //..

Applying KVL to collector-side loop,

$V_{cc} = I_c R_c + V_{CB}$

$\Rightarrow V_{CB} = V_{cc} - I_c R_c = 18 - 4.87\times10^{-3}\times 1.2\times10^{3}$

$V_{CB} = 12.16V$

(5) A transistor has $\alpha = 0.9$. If $I_E = 10mA$, find β, γ, I_B & I_c

Sol: Given $\alpha = 0.9$, $I_E = 10mA$.

$\beta = \frac{\alpha}{1-\alpha} = \frac{0.9}{1-0.9} = 9$ //..

$\gamma = 1 + \beta = 10$ //..

$I_C = \alpha I_E = 0.9 \times 10mA = 9mA$ //

$I_B = I_E - I_C = 10 \times 10^{-3} - 9 \times 10^{-3} = 1mA$ //

(6) Calculate α_{dc} & β_{dc} for the transistor, if $I_C = 1mA$. $I_B = 25\mu A$. Determine the new base current to give $I_C = 5mA$.

Sol: Given $I_C = 1mA$, $I_B = 25\mu A$, $\alpha_{dc} = ?$, $\beta_{dc} = ?$

$I_B' = ?$, $I_C' = 5mA$

Where, $\beta_{dc} = \frac{I_C}{I_B} = \frac{1 \times 10^{-3}}{25 \times 10^{-6}}$

$\boxed{\beta_{dc} = 40}$ //

Now, $\alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}} = \frac{40}{1+40}$

$\boxed{\alpha_{dc} = 0.975}$ //

We have $I_C' = \beta_{dc} I_B'$

$\Rightarrow I_B' = \frac{I_C'}{\beta_{dc}}$

$= \frac{5 \times 10^{-3}}{40}$

$\boxed{I_B' = 0.125mA}$ //

Syllabus: BJT Biasing : DC load line & Bias Point, Base bias, voltage divider bias. Numerical examples as applicable

* Transistor biasing (or) Biasing the transistor :

The process of applying external dc voltage to a transistor is called transistor biasing (or) biasing the transistor

(or)

The process of applying external dc voltage to a transistor to operate it in the desired region is called transistor biasing

(or)

The process of applying external dc voltage to a transistor to establish the required dc currents and voltages so that it operates in the appropriate region of the characteristics is called transistor biasing

(or)

The proper flow of zero signal collector current & the maintenance of proper collector-emitter voltage during the passage of signal is known as transistor biasing

Note:

① For transistor to be an amplifier: It must be operated in the active region of its characteristics (ie For CB configuration, base-emitter junction should be forward biased & collector-base junction should be reverse biased)

② For transistor to be a switch: It is operated in the cut-off region (open switch) and/or Saturation region (closed switch).

③ The circuit which provides transistor biasing is known as biasing circuit.

④ The basic conditions for faithful amplification (conditions for proper biasing of a transistor)

(i) Proper zero signal collector current.
(ii) Minimum proper base-emitter voltage (V_{BE}) at any instant. (0.3V for Ge & 0.7V for Si)
(iii) Minimum proper collector-emitter voltage (V_{CE}) at any instant. (0.5V for Ge & 1V for Si)

⑤ Need for biasing:

(i) To turn on the device
(ii) To set a fixed level of current & fixed voltage drop across the transistor junctions.
(iii) To operate transistor in the desired region (where it operates linearly & provides a constant voltage gain)

⑥ Inherent variations of transistor parameters:

In practice, the transistor parameters such as β, V_{BE} are not same for every transistor even of the same type. Ex: For BC147 (Silicon npn transistor), β varies from 100 to 600 (for one transistor it may be 100, for the other it may be 600).

The inherent variations of transistor parameters may change the operating point, resulting in unfaithful amplification. Therefore, the biasing network (circuit) is designed such that it should be able to work with all transistors of one type. In other words, the operating point should be independent of transistor parameters variations.

⑦ Stabilization:

The process of making operating point independent of temperature changes (or) Variations in transistor parameters is known as Stabilization.

⑧ Need for Stabilization: (or) Factors affecting Stability of Q-Point:

Stabilization of the operating point @ Q-Point is necessary due to the following reasons:

ⓐ Temperature dependence of I_c

The Collector leakage current (I_{CBO}) is greatly influenced (especially in Ge transistor) by temperature changes.

ⓑ Inherent Variations of transistor parameters:

The values of β & V_{BE} are not same for any two transistors even of the same type. Also V_{BE} decreases with increase in temperature.

ⓒ Thermal runaway:

The self-destruction of an unstabilized transistor is known as thermal runaway.

The Collector leakage current I_{CBO} is strongly dependent on temperature.

⑨ Stability factor:

The rate of change of collector current (I_c) w.r.t the reverse saturation current (I_{CBO} (or) I_{CO}) at constant β & I_B is called Stability factor (S)

ie $$S = \frac{dI_c}{dI_{co}} \text{ at constant } I_B \& \beta \quad \text{—} (*)$$

DC Load line and Bias Point :

DC Load line :

Defn: A Straight line drawn on the transistor output characteristics is called DC load line for a transistor circuit. (or)

The Load line is a graph of collector current (I_c) versus collector-emitter voltage (V_{CE}), for a given value of collector resistance (R_c) and a given supply voltage (V_{cc}) [For a common emitter circuit]

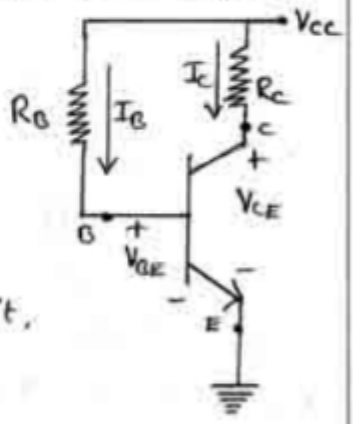
(or)

A Straight line which shows all corresponding values of I_c and V_{CE} that can exist in a particular circuit is called DC load line [For CE circuit]

Analysis:

Consider a npn CE transistor as shown in fig ①

Here Supply voltage (V_{cc}) forward biases the base-emitter junction & reverse biases the collector-emitter junction.



Fig①: npn CE transistor

Applying KVL to the collector circuit,

$$V_{cc} - I_c R_c - V_{CE} = 0 \quad -①$$

Case(i): Let $I_c = 0$

Eqn① becomes,

$$\boxed{V_{CE} = V_{cc}} \quad -②$$

Mark Point A as

$A(V_{CE}, I_c) = A(V_{cc}, 0)$

(Transistor in cut-off)

Case(ii): Let $V_{CE} = 0$

Eqn① becomes

$$\boxed{I_c = \frac{V_{cc}}{R_c}} \quad -③$$

Mark Point B as

$B(V_{CE}, I_c) = B(0, \frac{V_{cc}}{R_c})$ (Transistor in Saturation)

Now draw the Straight line through points A & B (DC load line)

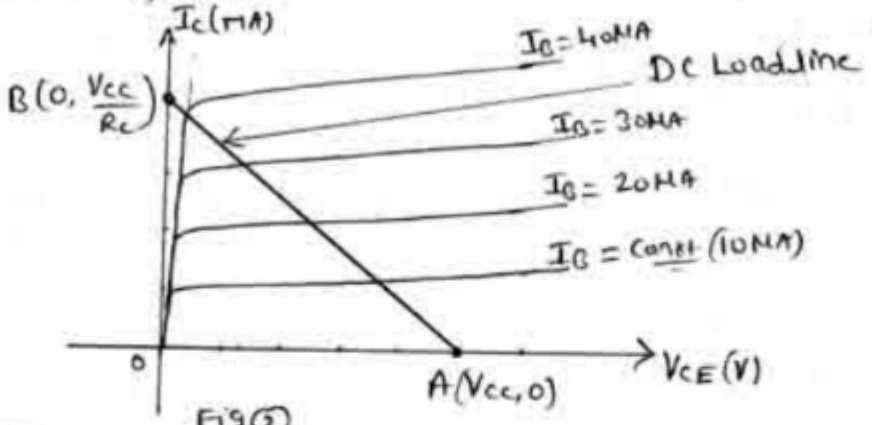


Fig (2)

Note:

Consider eqn (1)

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\Rightarrow I_C = \left(\frac{-1}{R_C}\right) V_{CE} + \left(\frac{V_{CC}}{R_C}\right) \quad \text{(or)} \quad \frac{V_{CE}}{(V_{CC})} + \frac{I_C}{(V_{CC}/R_C)} = 1$$

— (4) — (5)

Comparing (4) with $y = mx + c$ we get

$$m = -\frac{1}{R_C} \text{ (Slope)}$$

Comparing (5) with, $\frac{x}{a} + \frac{y}{b} = 1$, we get

$a = V_{CC}$, $b = V_{CC}/R_C$

(x-intercept) (y-intercept)

DC bias Point (or) operating Point (or) Quiescent Point (or) Q-Point (or) Silent Point

Defn: The point at which the dc load line intersects with the output characteristics of the transistor & it defines the dc conditions in the circuit is called dc bias Point.

(or)

The Point which identifies the transistor Collector

current & Collector-emitter voltage when there is no input signal at the base terminal is called dc bias Point. (or)

A Point on the DC load line which represents the zero signal values of V_{CE} (V_{CEQ}) & I_C (I_{CQ}) in a transistor is called dc operating Point (or) Q-Point.

Analysis:

Consider a npn CE transistor as shown in fig (2)

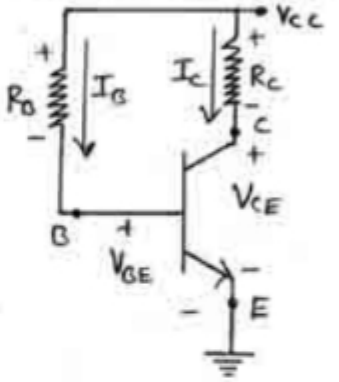


Fig (3): npn CE transistor

Step (1): Applying KVL to base loop.

$$V_{CC} - I_B R_B - V_{BE} = 0 \quad -(6)$$

$$\Rightarrow \boxed{I_B = I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B}} \quad -(7)$$

Step (2):

We have $\boxed{I_C = I_{CQ} = \beta I_B}$ $-(8)$

Step (3):

Applying KVL to Collector loop.

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\Rightarrow \boxed{V_{CE} = V_{CEQ} = V_{CC} - I_{CQ} R_C} \quad -(9)$$

Step (4):

Now Mark Q-Point as $Q(V_{CEQ}, I_{CQ})$

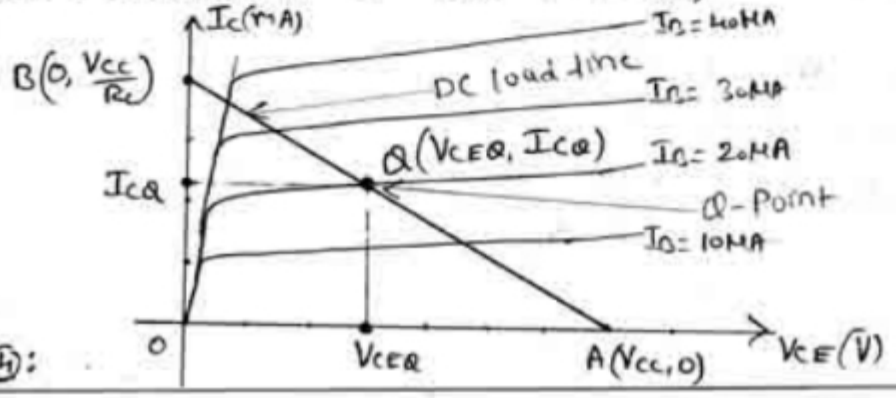


Fig (4):

Note:

① Consider dc load line drawn on CE output characteristics as shown in fig ⑤

→ Here Q_1 is near cut-off region, Q_5 is near saturation region & Q_3 is in the middle of the active region.

→ Selection of Q-point depend on the application of the transistor.

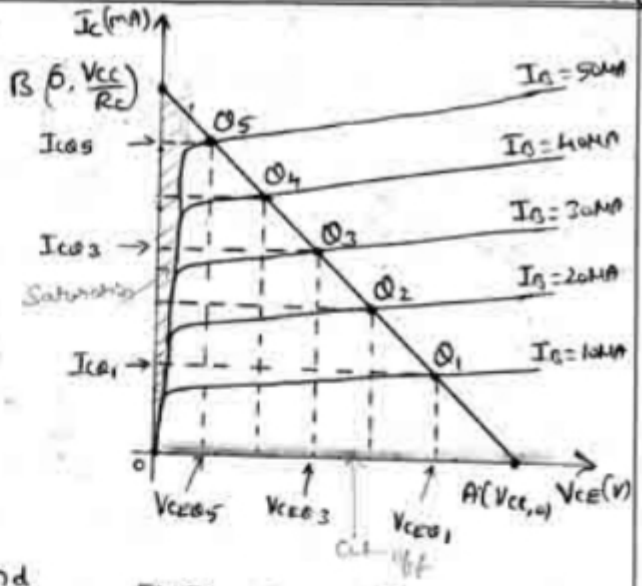


Fig ⑤ : CE output characteristics

② Variation of I_B, I_C & V_{CE} :

→ Here A (V_{CE}, I_C) = A (20V, 0mA)

B (V_{CE}, I_C) = B (0, 2mA)

→ Let us choose Q-Point as shown in fig ⑦.

Now from fig ⑦.

I_B = 20μA

I_C = 1mA

$V_{CE} = V_{CC} - I_C R_C$.

$= 20 - 1\times10^{-3}\times10\times10^{3}$

V_{CE} = 10V

⇒ At I_B = 20μA, Q (10V, 1mA)

→ When I_B is increased from 20μA to 40μA, I_C increases from 1mA to 1.95mA & V_{CE} decreases from 10V to 0.5V

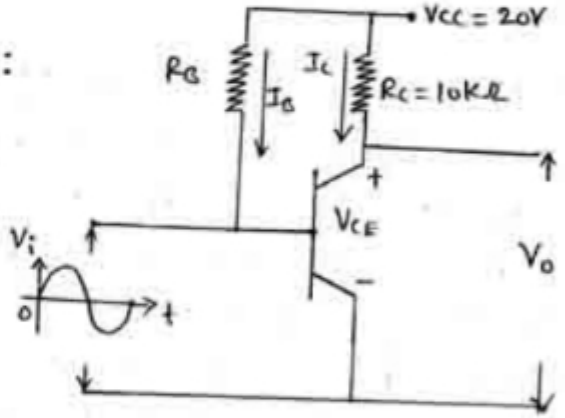


Fig ⑥ : CE npn transistor

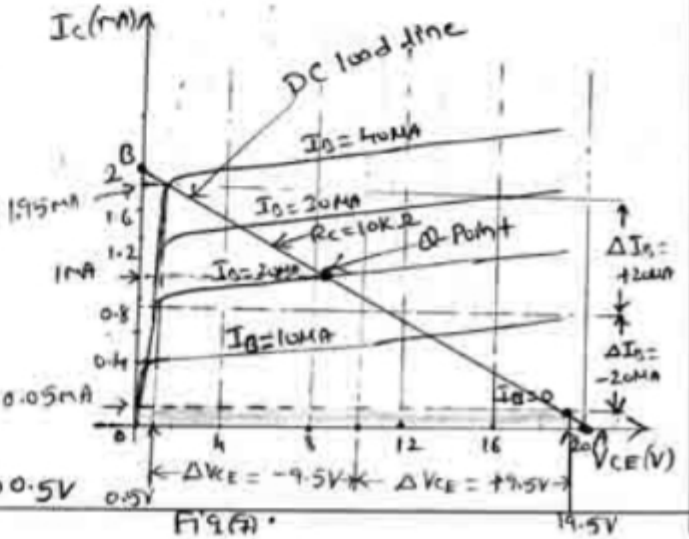


Fig ⑦.

→ When I_B is decreased from 20μA to 0

I_C decreases from 1mA to 0.05mA &

V_{CE} increases from 10V to 19.5V

∴ By varying input (V_i), I_B, I_C & V_{CE} can be varied

③ Selection of Q-Point: (For CE Configuration)

Based on the application of the transistor, it can be operated in any of the three regions such as,

ⓐ Saturation or near Saturation region

ⓑ Cut off region or near cut off region.

ⓒ Active region or at the centre of the active region or at the centre of the load line.

Fig ⑧ shows the input signal applied to base terminal.

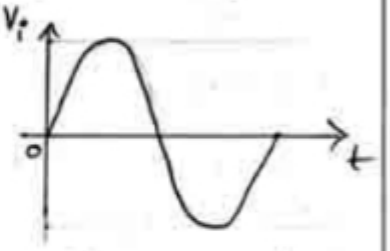


Fig ⑧: Input signal

④ Near Saturation region (Fig 9):

If Q-Point is located near the Saturation region, the transistor is driven into Saturation. Therefore the negative peak of the output voltage (positive peak of the output current) is clipped off. Here we get a distorted output.

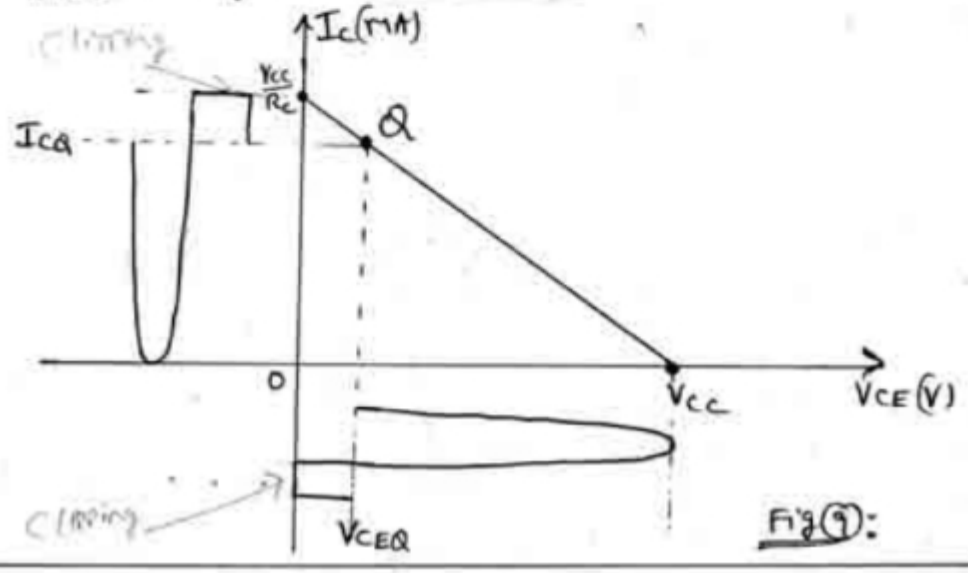


Fig ⑨:

(b) Near cut-off region (Fig 10)

If Q-point is located near the cut-off region, the transistor is driven into cut-off. Therefore the positive peak of the output voltage (negative peak of the output current) is clipped off. Here we get a distorted output.

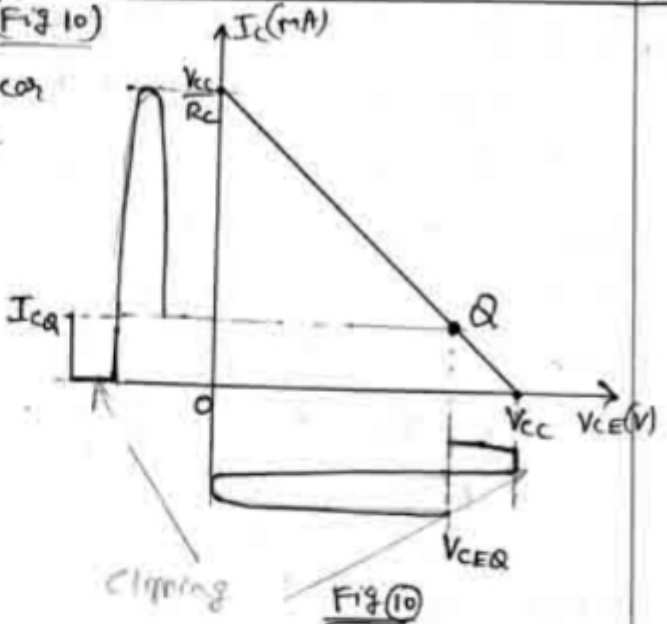


Fig (10)

(c) At the centre of the active region (Fig 11)

If Q-point is located at the centre of the load line (active region), the transistor is driven into active region. Here we get an undistorted output.

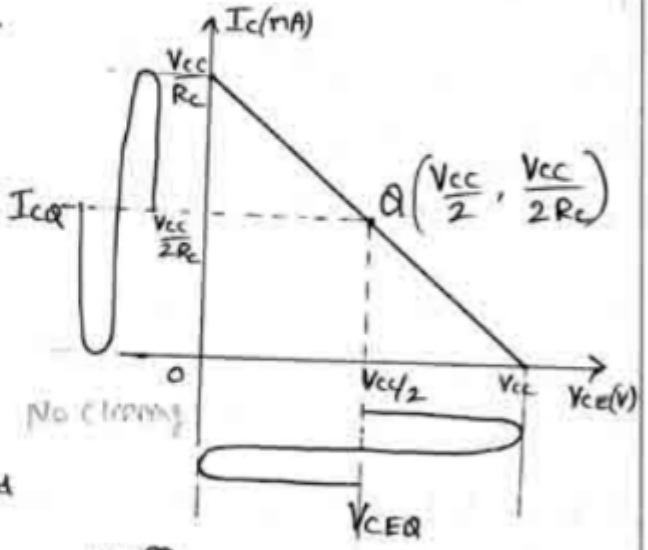


Fig (11)

Conclusion:

For a maximum undistorted output, the transistor should be driven into active region [or Q-Point must be located at the centre of the active region (load line)]

(d)

- For large-signal amplifiers, Q-Point must be at the centre of the load line (output voltage swing = ±10V)
- For small-signal amplifiers, Q-Point need not to be at the centre of the dc load line (output voltage swing not greater than ±1V)

(5) Effect of Emitter resistor :

⇒ Consider a circuit that has a resistor R_E as shown in fig (12)

Applying KVL to collector-emitter loop,

$$V_{cc} - V_{CE} - I_C R_E = 0 \quad (\because I_C \simeq I_E) \quad -(10)$$

Case (i) Put $V_{CE} = 0$

$$I_C = \frac{V_{cc}}{R_E} \quad -(11)$$

Mark as Point

$A(V_E, I_C) = (0, \frac{V_{cc}}{R_E})$

Case (ii): Put $I_C = 0$

$$V_{CE} = V_{cc} \quad -(12)$$

Mark as Point

$B(V_E, I_C) = (V_{cc}, 0)$

Draw a straight line through $A(0, \frac{V_{cc}}{R_E})$ & $B(V_{cc}, 0)$ to get dc load line (shown in fig 14)

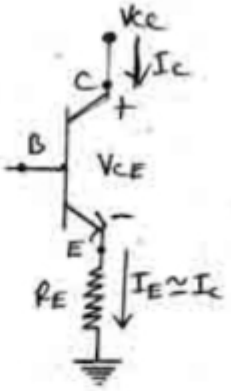


Fig (12)

$R_L(dc) = R_E$

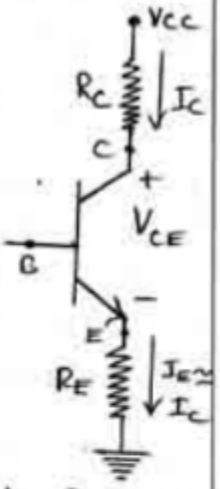


Fig (13)

$R_L(dc) = R_c + R_E$

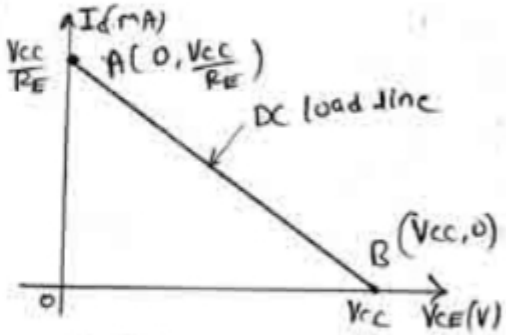


Fig (14):

⇒ Now consider a circuit that has Collector & Emitter resistors R_c & R_E as shown in fig (15).

Applying KVL to Collector-Emitter loop,

$$V_{cc} - I_C R_c - V_{CE} - I_C R_E = 0 \quad (\because I_C \simeq I_E) \quad -(13)$$

Case (i): Put $V_{CE} = 0$

$$I_C = \frac{V_{cc}}{R_c + R_E} \quad -(14)$$

Mark as Point

$A(0, \frac{V_{cc}}{R_c + R_E})$

Case (ii): Put $I_C = 0$

$$V_{CE} = V_{cc} \quad -(15)$$

Mark as Point

$B(V_{cc}, 0)$

Draw a straight line through A & B to get dc load line (fig 15)

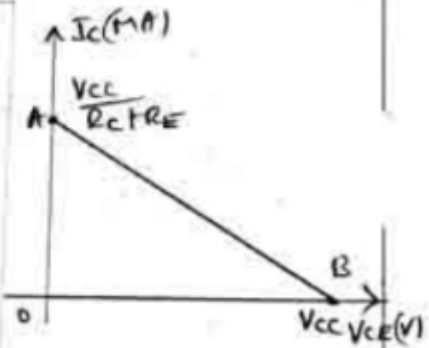


Fig (15):

* Methods of transistor biasing:

The most commonly used methods for biasing the transistors are

① Base bias ② Fixed bias ③ Fixed Current bias ④ Base resistor
② Emitter bias ⑤ Emitter feedback bias ⑥ Base bias with emitter feedback.
③ Collector-to-base bias ⑦ Collector feedback bias ⑧ Base bias with Collector feedback.
④ Voltage-divider bias ⑨ Self bias ⑩ Universal bias ⑪ Emitter current bias.

① Base bias ② Fixed bias ③ Fixed Current bias ④ Base Resistor

The circuit in which the base current is a constant quantity determined by supply voltage V_{CC} & base resistor R_B (constant quantities) is called Fixed bias

Fig ⑯ shows the base bias circuit.

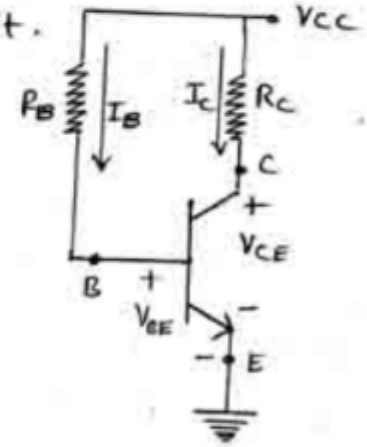


Fig ⑯: Base bias circuit

Step ①:
Applying KVL to base-emitter circuit,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$\Rightarrow \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}} \quad -⑯$$

Step ②:
We have,

$$\boxed{I_C = h_{FE} I_B} \quad -⑰$$

Step ③:
Applying KVL to Collector-emitter circuit.

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\Rightarrow \boxed{V_{CE} = V_{CC} - I_C R_C} \quad -⑱$$

When V_{CC}, R_C, R_B & h_{FE} are known, the values of I_B, I_C & V_{CE} can be determined using ⑯, ⑰ & ⑱

Note:

① Effect of $h_{FE(max)}$ & $h_{FE(min)}$: (For Base bias & Voltage divider)

When h_{FE} (β) is known, the circuit bias conditions (I_B, I_C & V_{CE}) can be determined exactly.

In practice the precise (exact) value of h_{FE} is not known. Therefore the maximum & minimum values of current gain (h_{FE}) can be obtained from the manufacturer data sheet. Now $h_{FE(max)}$ & $h_{FE(min)}$ must be used to calculate the range of I_C & V_{CE}.

Q-Point shifts from active region to saturation (when h_{FE} is increased to infinity), or cut-off (when h_{FE} is decreased to zero).

② Base bias using PnP transistor:

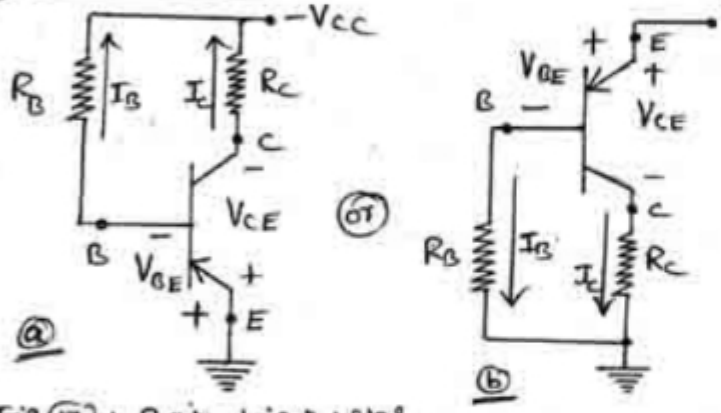


Fig (17): Base bias using a PnP transistor

→ Voltage Polarities & current directions are reversed compared to npn transistor.

→ Eqns (16), (17) & (18) are used to analyze the circuit.

③ Design of base-bias circuit:

Finding the component values of biasing circuit is called design.

Bias circuit design can be done either in mathematical approach or characteristics approach.

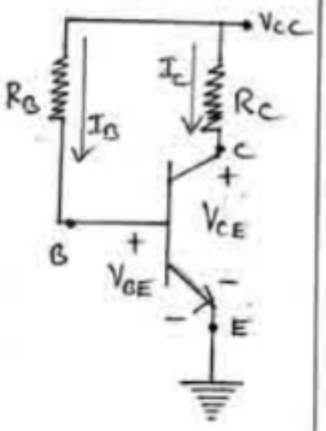
Mathematical approach:

The values of V_{CC}, V_{CE}, V_{BE}, I_C (or I_B) & h_{FE} will be given.

The design steps are as follows

Step 1: Calculate R_C using the relation

$$R_C = \frac{V_{CC} - V_{CE}}{I_{C_1}} \quad -(19)$$



Fig(18): Base-bias circuit

Step 2: Calculate I_B (or I_C) using the relation,

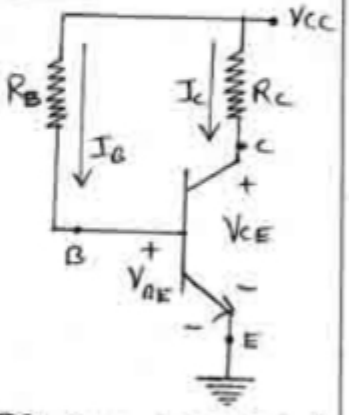
$$I_B = \frac{I_C}{h_{FE}} \quad (or) \quad I_C = h_{FE} I_B \quad -(20)$$

Step 3: Calculate R_B using the relation.

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} \quad -(21)$$

(5) DC load line & Q-point of Base-bias

⇒ Consider the base bias circuit as shown in fig(19)



Fig(19): Base bias circuit

Applying KVL to collector-emitter loop.

$$V_{CC} - I_C R_C - V_{CE} = 0 \quad -(22)$$

Put $I_C = 0$	Put $V_{CE} = 0$
$V_{CE} = V_{CC}$ -(23)	$I_C = \frac{V_{CC}}{R_C}$ -(24)

Point $A(V_{CC}, 0)$ Point $B\left(0, \frac{V_{CC}}{R_C}\right)$

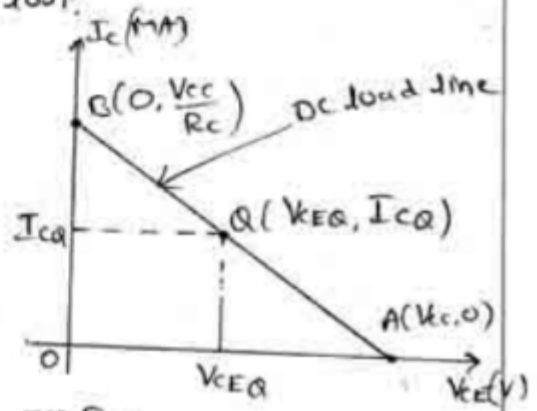
⇒ Applying KVL to base-emitter loop.

$$V_{CC} - I_B R_C - V_{BE} = 0 \quad -(25)$$

$$\Rightarrow I_B = I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} \quad -(26)$$

We have, $I_C = I_{CQ} = \beta I_B \quad -(27)$

From (22) $\therefore V_{CE} = V_{CEQ} = V_{CC} - I_{CQ} R_C \quad -(28)$



Fig(20):

⑤ Advantages, disadvantages & APPLICATIONS of Base bias

Advantages (or) Merits

① A very less number of components are required.

② Operating point can be shifted easily anywhere in the active region by simply changing the base resistor (R_B).

③ There is no loading of the source by the biasing circuit since no resistor is employed across base-emitter junction.

Disadvantages (or) Demerits (or) drawbacks

① Poor Stabilization (operating point is unstable)

② The stability factor is very high ($S = \beta + 1$), hence prone to thermal runaway.

APPLICATIONS (or) USAGE

① Rarely used in linear circuits (ie the circuits which uses the transistor as a current source).

② It is often used in circuits where transistor is used as a switch.

---

③ Voltage-divider bias (or) Self bias (or) universal bias (or) Emitter current bias:

Voltage divider bias is the most stable transistor bias circuit.

Circuit operation

→ A voltage divider bias circuit is shown in fig (21).

→ Resistors R_1 & R_2 divide the supply voltage V_{CC} & voltage drop across R_2 provides fixed bias voltage 'V_B' at the base.

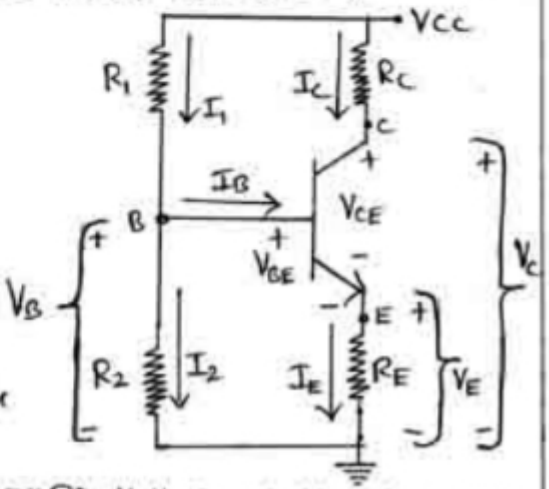


Fig (21): Voltage-divider bias circuit

→ The emitter resistor R_E provides Stabilization.

→ The total dc load in series with the transistor is $(R_C + R_E)$

→ Let the current I_2 is very much larger than I_B & V_B is assumed to be Constant.

Methods of Analysis

① Approximate Method ② Analysis

② Exact ② Accurate ② Precise Method ② Analysis

① Approximate Method : (Fig 21)

It is a direct method, Saves time & energy.

Applying KVL to Voltage-divider network,

$$V_{CC} - I_1 R_1 - I_2 R_2 = 0 \quad -(29)$$

$$\Rightarrow \boxed{I_2 = \frac{V_{CC}}{R_1 + R_2}} \quad -(30)$$

[Since $I_1 = I_B + I_2$
$\Rightarrow I_1 \simeq I_2$ $(\because I_2 >> I_B)$ $-(31)$]

Voltage across R_2

$$V_B = I_2 R_2 \quad -(32)$$

$$\boxed{V_B = \frac{V_{CC}}{R_1 + R_2} R_2} \quad -(33) \quad [\text{Using } (30) \text{ in } (32)]$$

We have, $V_B = V_{BE} + V_E \quad -(34)$

$$\Rightarrow \boxed{V_E = V_B - V_{BE}} \quad -(35)$$

Emitter current, $I_E = \frac{V_E}{R_E} \quad -(36)$ [Using (34) in (36)]

$$\boxed{I_E = \frac{V_B - V_{BE}}{R_E}} \quad -(37)$$

Applying KVL to Collector loop,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\Rightarrow \boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)} \quad -(38) \quad [\because I_E \simeq I_C]$$

Collector Voltage,

$$V_C = V_{CC} - I_C R_C \text{ (or) } V_{CE} + V_E \quad -(39)$$

With I_C & I_E constant, the V_{CE} remains constant. Q-Point is independent of h_{FE} (∵ h_{FE} is not involved in any of the above equations)

(2) Exact (or) Accurate (or) Precise Method:

It can be applied to any voltage divider circuit.

The voltage-divider network is replaced by its Thevenin equivalent circuit.

Consider the voltage divider bias circuit as shown in fig (22).

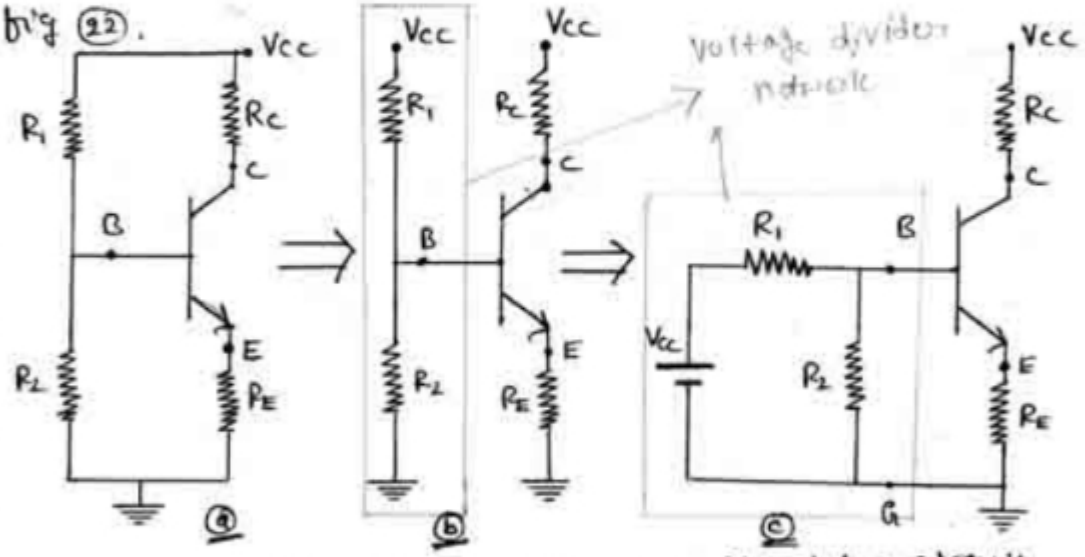


Fig (22): Simplification of voltage divider bias circuit

Now consider the voltage divider network as shown in fig (23)

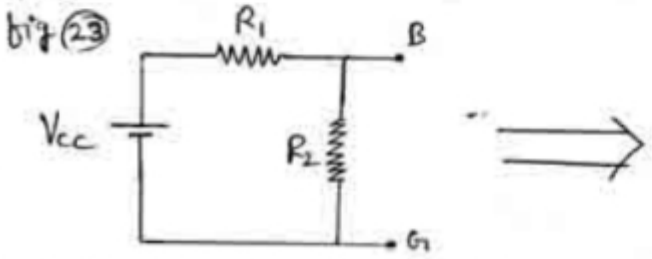


Fig (23): Voltage divider network

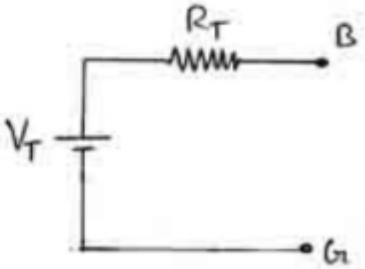


Fig (24): Thevenin equivalent circuit

The Thevenin equivalent circuit of voltage divider network is shown in fig (24).

V_T: Thevenin's voltage:

V_T is the voltage across B-G terminals or voltage across R_2.

From voltage divider rule,

$$V_T = \frac{V_{CC} R_2}{R_1 + R_2} \quad -(40)$$

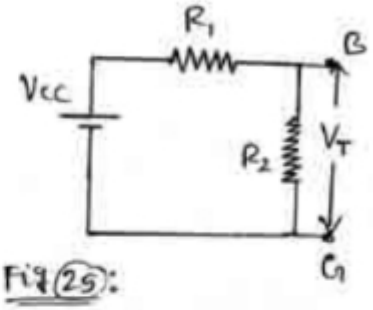


Fig (25):

R_T: Thevenin's resistance:

R_T is the resistance seen between the terminals B-G. (By shorting the voltage source Vcc)

$$\therefore R_T = \frac{R_1 R_2}{R_1 + R_2} \quad -(41)$$

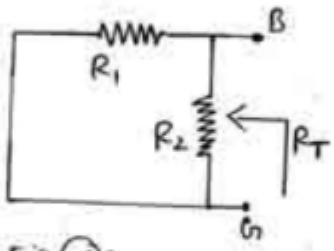


Fig (26):

Now replace the voltage divider network with its Thevenin equivalent circuit (between B & G) as shown in fig (27)

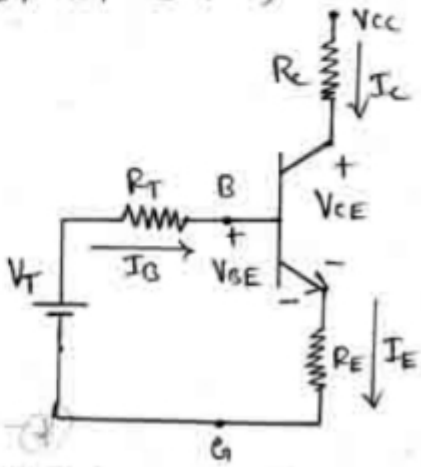


Fig (27): Voltage divider bias circuit with Thevenin equivalent circuit

Applying KVL to base-emitter loop,

$$V_T - I_B R_T - V_{BE} - I_E R_E = 0$$

$$\Rightarrow V_T - V_{BE} = I_B R_T + I_E R_E$$

$$\Rightarrow V_T - V_{BE} = I_B R_T + (I_B + I_C) R_E$$

$$\Rightarrow V_T - V_{BE} = I_B R_T + (I_B + h_{FE} I_B) R_E$$

$$\Rightarrow V_T - V_{BE} = I_B [R_T + R_E (1 + h_{FE})]$$

$$\Rightarrow I_B = \frac{V_T - V_{BE}}{R_T + R_E (1 + h_{FE})} \quad -(42)$$

Now $\boxed{I_C = h_{FE} I_B}$ —(43)

Applying KVL to Collector - emitter loop,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\Rightarrow \boxed{V_{CE} = V_{CC} - I_C R_C - I_E R_E} \quad -(44)$$

Emitter Voltage, $\boxed{V_E = I_E R_E}$ —(45)

Collector Voltage, $\boxed{V_C = V_{CE} + V_E \text{ (or) } V_{CC} - I_C R_C}$ —(46)

Base Voltage, $\boxed{V_B = V_{BE} + V_E}$ —(47)

Q-Point is independent of h_{FE} (though h_{FE} is used in the above equations)

Note:

① Q-Point (or) operating point is almost independent of $h_{FE}(\beta)$ variation. So voltage divider bias is the most stable transistor bias circuit. (See Numerical 15.4.4)

② Voltage divider bias using PnP transistor:

→ Voltage Polarities & current directions are reversed compared to npn transistor.

→ A PnP transistor voltage divider bias circuit is analyzed in exactly the same way as an npn transistor voltage divider bias circuit.

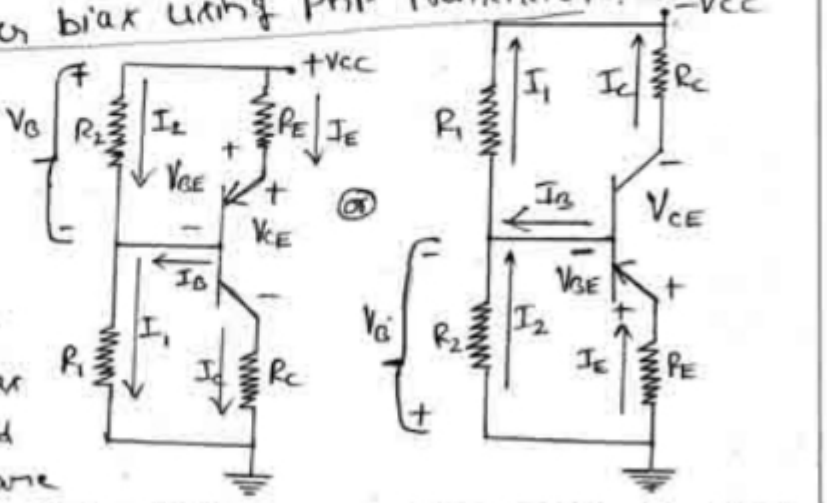


Fig (28): PnP transistor Voltage Divider bias circuit

③ The stability of a system (transistor circuit) is a measure of sensitivity of a network to variations in its parameters.

In any transistor amplifier, I_C is sensitive to the following parameters.

β: Increases with increase in temperature.

V_{BE}: Decreases about 7.5mV/°C increase in temp

I_{CO} (Reverse Saturation Current): Doubles for every 10°C increase in temperature

Design of voltage-divider bias circuit: (Finding R_1, R_2 R_C & R_E)

The values of V_{CC}, V_{CE}, V_{BE}, I_C & h_{FE} will be given.

The design steps are as follows:

Step 1: Let $$I_2 = \frac{I_C}{10} \quad -(48)$$ (As a thumb rule)

Step 2: Let $V_E >> V_{BE}$ (If V_E is not given) $-(49)$

Choose V_E in 3V-5V range (3V when V_{CC} is low (9V), 5V regardless of voltage)

Step 3: Calculate R_E using the relation,

$$R_E = \frac{V_E}{I_C} \quad (\because I_C \simeq I_E) \quad -(50)$$

Step 4: Calculate R_2 using the relation

$$R_2 = \frac{V_B}{I_2} \quad -(51)$$

where, $V_B = V_{BE} + V_E \quad -(52)$

Step 5: Calculate R_1 using the relation,

$$R_1 = \frac{V_{CC} - V_B}{I_2} \quad -(53)$$

Step 6: Calculate R_C using the relation.

$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} \quad -(54)$$

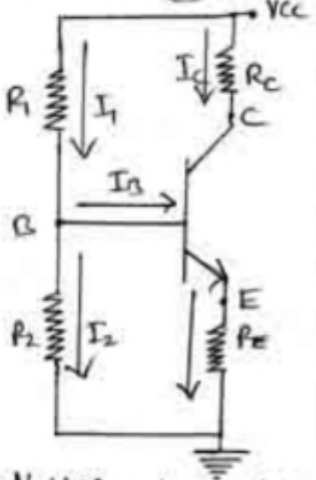


Fig (29): Voltage-divider bias circuit

(5) DC load line & Q-Point of Voltage-divider bias

⇒ Consider the voltage-divider bias circuit as shown in fig (30)

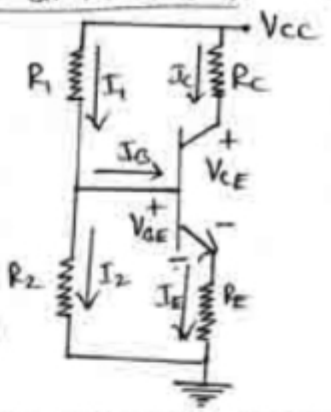


Fig (30): Voltage-divider bias circuit

Applying KVL to collector-emitter loop,

$$V_{CC} - V_{CE} - I_C R_C - I_E R_E = 0$$

$$\Rightarrow V_{CC} - V_{CE} - I_C (R_C + R_E) = 0 \quad (\because I_C \simeq I_E) \quad -(55)$$

Put $I_C = 0$	Put $V_{CE} = 0$
$V_{CE} = V_{CC}$ —(56)	$I_C = \frac{V_{CC}}{R_C + R_E}$ —(57)
Point A(V_{CC}, 0)	Point B$\left(0, \frac{V_{CC}}{R_C + R_E}\right)$

⇒ We have

$I_E \doteq \frac{V_B - V_{BE}}{R_E}$ where, $V_B = \frac{V_{CC} R_2}{R_1 + R_2}$

& $I_C = I_{CQ} \simeq I_E$ — (58)

Also $V_{CE} = V_{CEQ} = V_{CC} - I_C(R_C + R_E)$ —(59)

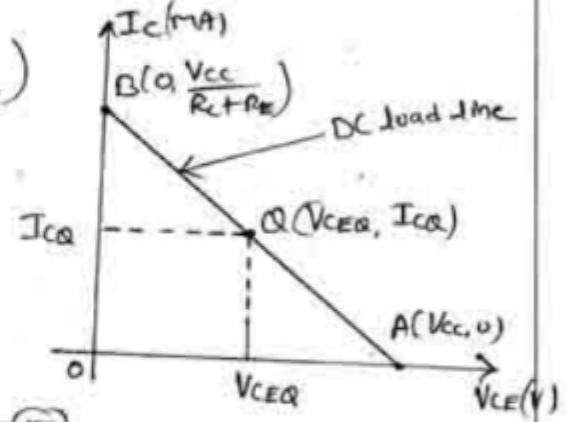


Fig (31)

(6) Which value of β to be used?

(a) Distinct β_{min} & β_{max} given	(b) Range of β given ($\beta_{min} - \beta_{max}$)
Solve using β_{min} & β_{max} separately	GM or geometric average of the two values should be used. $\beta = \sqrt{\beta_{min} \times \beta_{max}}$

(7) Why Si is preferred over Ge?

Main reasons

(a) Smaller I_{CBO} : Si: 0.01 nA to 1 nA (At 25°C)
Ge: 2 to 15 nA

(b) Smaller variation of I_{CBO} with temperature:

For Si: I_{CBO} approximately doubles with each 12°C rise
For Ge: I_{CBO} approximately doubles with each 8 to 10°C rise.

(c) Greater working temperature:
For Si: Normal working temperature upto 150°C
For Ge: Normal working temperature upto 70°C.

(d) Higher PIV rating:
Si: PIV ratings around 1000V
Ge: PIV ratings around 400V.

[One drawback of Si as compared to Ge is potential barrier of Si diode is 0.7V: which is more than that of Ge diode (0.3V)]

(8) Advantages, disadvantages & Applications of Voltage-divider bias

Advantages or Merits:
① Operating Point (Q-Point) is almost independent of β (h_{FE}) variation.
② The Stability factor is the smallest possible value, ($S \simeq 1$) hence leads to the maximum possible thermal Stability. ③ Operating Point stabilized against shift in temperature.

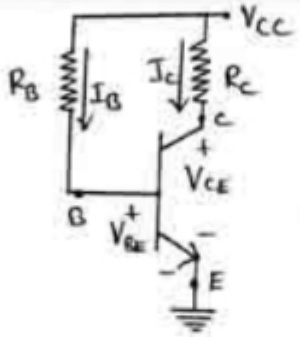
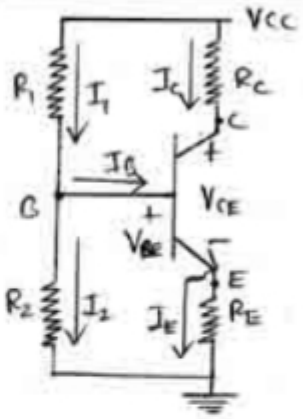
Disadvantages or Demerits or drawbacks
① It is complex, since it requires more components than other biasing circuits.
② If R_E is of large value, high V_{cc} is necessary. This increases cost as well.
③ The negative feedback caused by R_E, reduces the

gain of the amplifier.

Applications @ Usage

① Used to biax linear amplifier

② Comparision of Baxing Circuits

Sl no.	Parameter	Base biax	Voltage divider biax
1	Circuit		
2	Stability	Poor	Excellent
3	Biax Conditions	UnPredictable	Most Predictable
4	Feedback	Not Present	Negative feedback
5	components (Circuit Complexity)	Less	More
6	Stability Factor(S)	$S = 1 + \beta$ @ $1 + h_{FE}$	$S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E + R_{TH}}\right)} \simeq 1$ Where $R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$
7	V_{CE} (min)	1.8 V	9.4 V
8	V_{CE}(max)	13.75V	10.4 V
9	I_C	$= \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right)$	$= \frac{\frac{V_{CC} R_2}{R_1 + R_2} - V_{BE}}{R_E}$

10	V_{CE}	$= V_{cc} - I_c R_c$	$= V_{cc} - I_c (R_c + R_E)$
11	DC Load line	A Straight line from $A(V_{cc}, 0)$ to $B(0, \frac{V_{cc}}{R_c})$	Straight line from $A(V_{cc}, 0)$ to $B(0, \frac{V_{cc}}{R_c + R_E})$
12	Q-Point	$Q(V_{CEQ}, I_{CQ})$ $V_{CEQ} = V_{cc} - I_{CQ} R_c$ $I_{CQ} = \left(\frac{V_{cc} - V_{BE}}{R_B}\right)\beta$	$Q(V_{CEQ}, I_{CQ})$ $V_{CEQ} = V_{cc} - I_c (R_c + R_E)$ $I_{CQ} = \frac{\frac{V_{cc} R_2}{R_1 + R_2} - V_{BE}}{R_E}$
13	Applications	Used in Switching circuits	Used in linear amplifier

① Draw the dc load line for the circuit shown in fig ①ⓐ

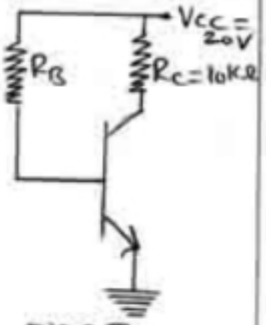
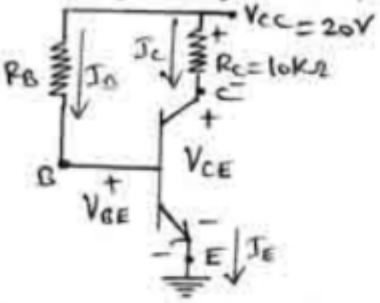


Fig ①ⓐ

sol: Given circuit is redrawn below.



Applying KVL to collector - emitter loop,

$$V_{cc} - I_c R_c - V_{CE} = 0$$

Put $I_c = 0$

$$V_{CE} = V_{cc} = 20V$$

Mark as Point

$A(V_{CE}, I_c) = A(20, 0)$

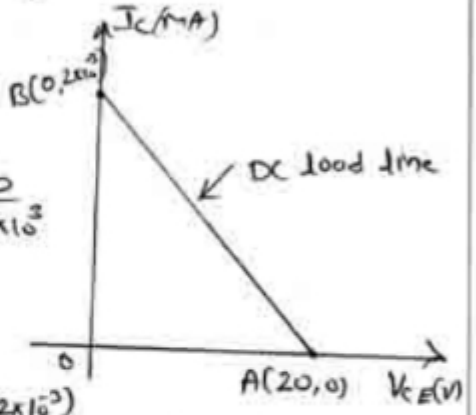
Put $V_{CE} = 0$

$$I_c = \frac{V_{cc}}{R_c} = \frac{20}{10 \times 10^3}$$

$$I_c = 2mA$$

Mark as Point

$B(V_{CE}, I_c) = B(0, 2 \times 10^{-3})$



Draw a straight line through A(20, 0) & B(0, 2×10^{-3}) to get load line

② The transistor circuit in fig 2ⓐ has the collector characteristics shown in fig 2ⓑ. Determine the circuit Q-Point & estimate the maximum symmetrical output voltage swing.

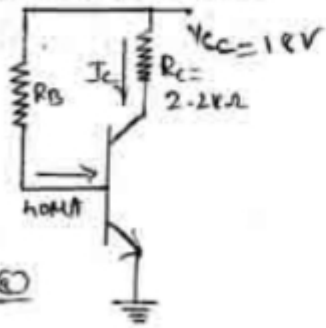


Fig 2ⓐ

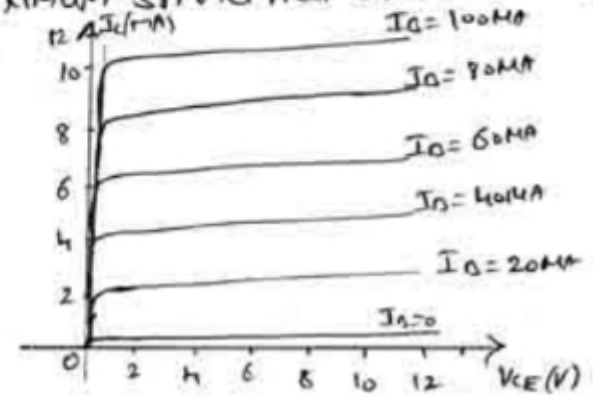


Fig 2ⓑ

sol: Applying KVL to collector - emitter loop,

$$V_{cc} - I_c R_c - V_{CE} = 0$$

Put $I_C = 0$

$V_{CE} = V_{cc} = 18V$

Point A(18, 0)

Put $V_{CE} = 0$

$I_C = \frac{V_{cc}}{R_c} = \frac{18}{2.2 \times 10^3}$

$I_C = 8.18mA$

Point B$(0, 8.18 \times 10^{-3})$

Draw the dc load line through points A & B on the given output-characteristics [fig 2(b)].

The intersection of the dc load line & $I_B = 40\mu A$ characteristic is Q-point as shown in fig 2©.

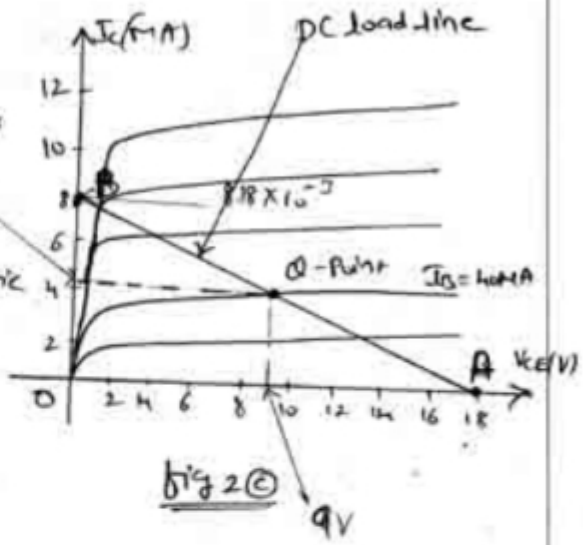


fig 2©

The dc bias conditions are

$I_C \simeq 4.1mA$ & $V_{CE} \simeq 9V$

∴ Maximum Symmetrical output voltage swing is,

$\boxed{\Delta V_{CE} \simeq \pm 9V}$ //

③ The base bias circuit is shown in fig 3(a). Determine I_B, I_C & V_{CE}.

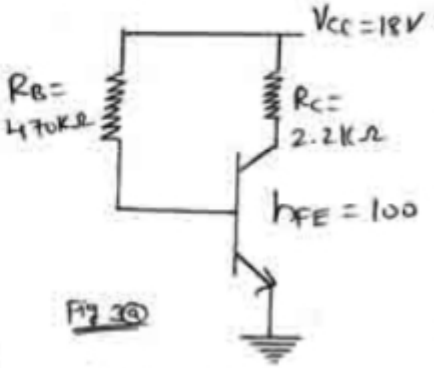
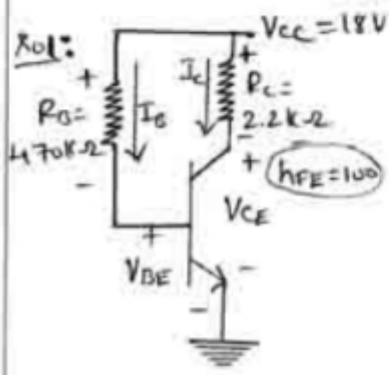


fig 3@

Sol:



Applying KVL to base-emitter circuit,

$V_{cc} - I_B R_B - V_{BE} = 0$

$\Rightarrow I_B = \frac{V_{cc} - V_{BE}}{R_B} = \frac{18 - 0.7}{470 \times 10^3} = 36.8\mu A$

$V_{BE} = 0.3V$ for Ge
$V_{BE} = 0.7V$ for Si
If V_{BE} not given take $V_{BE} = 0.7V$

We have, $I_C = h_{FE} I_B = 100 \times 36.8 \times 10^{-6} = 3.68\,mA$

Applying KVL to collector-emitter loop,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_C R_C = 18 - 3.68 \times 10^{-3} \times 2.2 \times 10^{3}$$

$$\boxed{V_{CE} = 9.904\,V}$$

4) For the circuit shown in fig 4(a), draw DC load line & mark the Q-Point. Assume $\beta = 100$ & neglect V_{BE}

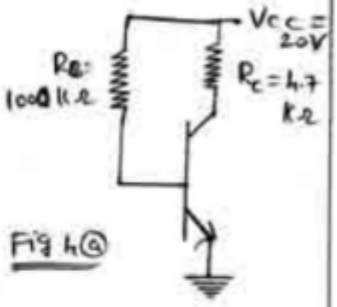
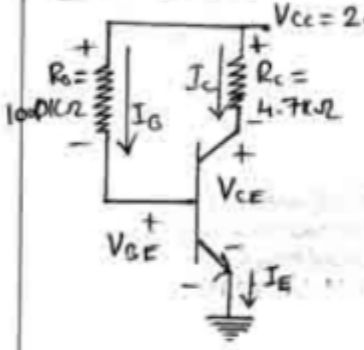


Fig 4(a)

Sol:

DC load line



Step 1: Applying KVL to collector loop,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

Step 2: Put $I_C = 0$, $V_{CE} = V_{CC} = 20V$

Mark as Point A(V_{CE}, 0) = A(20, 0)

Step 3: Put $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C} = \frac{20}{4.7 \times 10^{3}} = 4.25\,mA$

Mark as Point B(I_C, 0) = B(4.25×10^{-3}, 0)

Step 4: Draw a straight line through Points A & B, as shown in fig 4(b)

Q-Point

Step 1: Applying KVL to base-emitter loop,

$$V_{CC} - I_B R_B - V_{BE} = 0 \quad (\text{Given } V_{BE} = 0)$$

$$\Rightarrow I_B = \frac{V_{CC}}{R_B} = \frac{20}{1 \times 10^{6}} = 20\,\mu A$$

We have

$$I_{CQ} = I_C = \beta I_B = 100 \times 20 \times 10^{-6} = 2\,mA$$

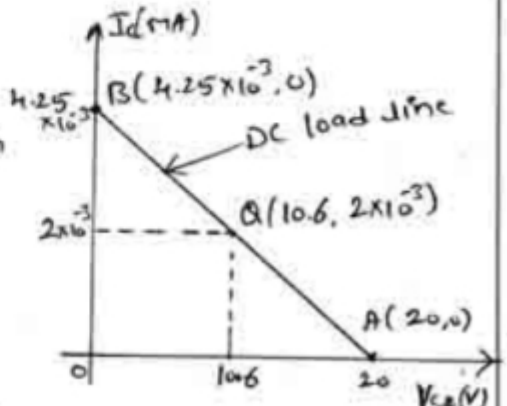


Fig 4(b)

Step 2: KVL to collector-emitter loop,

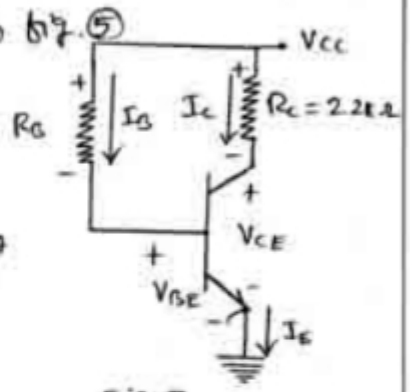
$V_{cc} - I_c R_c - V_{CE} = 0$

$\Rightarrow V_{CEQ} = V_{CE} = V_{cc} - I_c R_c = 20 - 2\times10^{-3} \times 4.7\times10^{3} = 10.6V$

Mark as Point Q(10.6, 2×10^{-3}) [Shown in fig 4(b)]

(5) Calculate the value of R_B that will saturate the base bias transistor circuit. Given $h_{FE} = 200$, $V_{CE} = 0.3$ V $R_c = 2.2K\Omega$, $V_{cc} = 10V$

Sol: The base-bias circuit is shown in fig.(5)



Fig(5)

Applying KVL to collector-emitter loop.

$V_{cc} - I_c R_c - V_{CE} = 0$

$\Rightarrow I_c = \frac{V_{cc} - V_{CE}}{R_c} = \frac{10 - 0.3}{2.2\times10^{3}} = 4.409$ mA

We have,

$I_C = h_{FE} I_B$

$\Rightarrow I_B = \frac{I_c}{h_{FE}} = \frac{4.409\times10^{-3}}{200}$

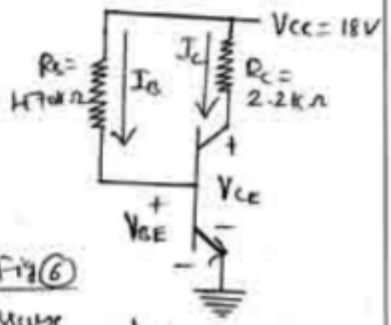
$I_B = 22.04\mu A$//.

APPLying KVL to base-emitter loop.

$V_{cc} - I_B R_B - V_{BE} = 0$ (Assume $V_{BE} = 0.7V$)

$\Rightarrow R_B = \frac{V_{cc} - V_{BE}}{I_B} = \frac{10 - 0.7}{22.04\times10^{-6}} = 421.96K\Omega$

(6) Calculate the maximum & minimum levels of I_c & V_{CE} for the base bias circuit shown in fig(6) when $h_{FE(min)} = 50$ & $h_{FE(max)} = 200$.



Fig(6)

Sol: KVL to base loop.

$V_{cc} - I_B R_B - V_{BE} = 0$

$\Rightarrow I_B = \frac{V_{cc} - V_{BE}}{R_B} = \frac{18 - 0.7}{470\times10^{3}} = 36.8\mu A$ (Assume, $V_{BE} = 0.7V$)

For $h_{FE(min)}$

$I_C = h_{FE(min)} I_B$

$= 50 \times 36.8 \times 10^{-6}$

$I_C = 1.84\ mA$

$V_{CE} = V_{CC} - I_C R_C$

$= 18 - 1.84 \times 10^{-3} \times 2.2 \times 10^{3}$

$= 13.95\ V$

For $h_{FE(max)}$

$I_C = h_{FE(max)} I_B$

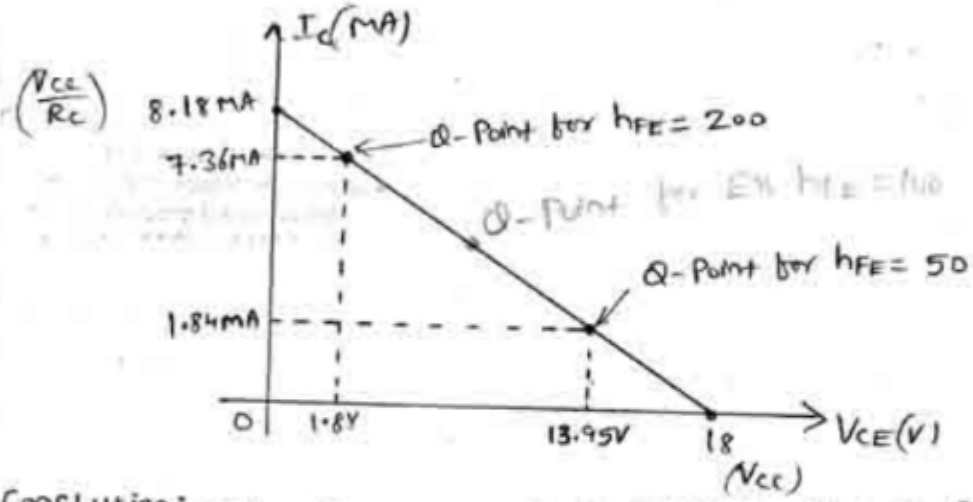
$= 200 \times 36.8 \times 10^{-6}$

$= 7.36\ mA$

$V_{CE} = V_{CC} - I_C R_C$

$= 18 - 7.36 \times 10^{-3} \times 2.2 \times 10^{3}$

$= 1.8\ V$



Conclusion:
- From the above characteristics, the Q-Point changes when β (h_{FE}) changes.
- Q-Point shifts towards Saturation region (from active region) when h_{FE} is increased from 100 to 200
- Q-Point shifts towards Cut-off region (from active region) when h_{FE} is decreased from 100 to 50.

3) Determine the following for the fixed-bias configuration of fig ④.

ⓐ I_{BQ} & I_{CQ} ⓔ Stability factor

ⓑ V_{CEQ}

ⓒ V_B & V_C ⓓ V_{BC}. ⓔ Saturation level

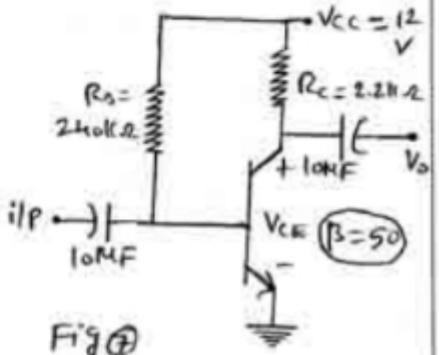


Fig ④

Q) Neglect capacitors.

(a) Applying KVL to base-emitter loop.

$V_{CC} - I_B R_B - V_{BE} = 0$

$\Rightarrow I_B = I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B}$

$\Rightarrow I_{BQ} = \frac{12 - 0.7}{240 \times 10^3}$

$\boxed{I_{BQ} = 47.08\,\mu A}$

We have, $I_{CQ} = \beta I_{BQ}$

$= 50 \times 47.08 \times 10^{-6}$

$\boxed{I_{CQ} = 2.35\,mA}$ //

(b) KVL to collector-emitter loop

$V_{CC} - I_C R_C - V_{CE} = 0$

$\Rightarrow V_{CE} = V_{CC} - I_C R_C$

$V_{CEQ} = V_{CE} = 12 - 2.35 \times 10^{-3} \times 2.2 \times 10^3$

$\boxed{V_{CEQ} = 6.83\,V}$ //

(c) $\boxed{V_B = V_{BE} = 0.7V}$

$\boxed{V_C = V_{CE} = 6.83V}$ //

(d) $V_{BC} = V_B - V_C = 0.7 - 6.83 = -6.13V$

(e) Saturation level (a) Saturation Current.

$I_{C_{Sat}} = \frac{V_{CC}}{R_C} = \frac{12}{2.2 \times 10^3} = 5.45\,mA$ //

(f) Stability factor

$S = 1 + \beta = 51$

(g) $V_{CE(cut-off)} = V_{CC} = 12V$

(8) Fig (8) shows biasing with base resistor method.

(i) Determine I_C & V_{CE}, Neglect small base-emitter voltage. Given $\beta = 50$

(ii) If R_B is changed to 50KΩ, find the new operating point

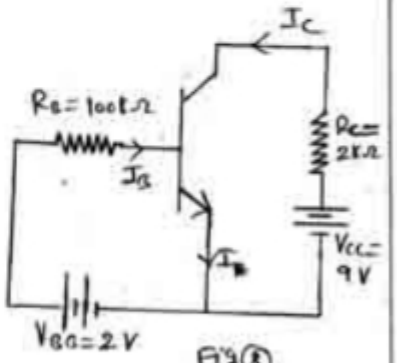


Fig (8)

(i)

Applying KVL to base loop,

$V_{BB} - I_B R_C - V_{BE} = 0$ —(1)

$\Rightarrow I_B = \frac{V_{BB}}{R_B} = \frac{2}{100 \times 10^3} = 20\,\mu A$ (Given $V_{BE} = 0$)

Now $I_C = \beta I_B = 50 \times 20 \times 10^{-6} = 1\,mA$ //

Applying KVL to collector loop.

$V_{CC} - I_C R_C - V_{CE} = 0$ —(2)

$\Rightarrow V_{CE} = V_{CC} - I_C R_C = 9 - 1\times10^{-3} \times 2\times10^{3} = \underline{7V}$

(ii) From (1), $I_B = \frac{V_{BB}}{R_B} = \frac{2}{50\times10^{3}} = 40\mu A$

Now, $I_C = \beta I_B = 50 \times 40\times10^{-6} = 2mA$ //.

& $V_{CE} = V_{CC} - I_C R_C = 9 - 2\times10^{-3} \times 2\times10^{3} = 5V$ //.

∴ New operating point is (5V, 2mA)

(9) Design base resistor bias circuit for $V_{CE} = 8V$ & $I_C = 2mA$. Given $V_{CC} = 15V$, $\beta = 100$ (Si transistor), $V_{BE} = 0.6V$. Also calculate the load resistance.

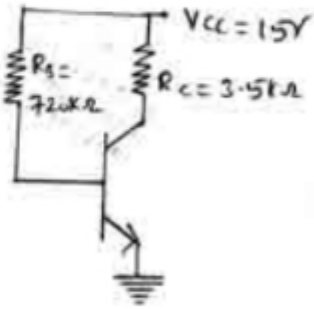
(10) Given $V_{CE} = 8V$, $I_C = 2mA$, $V_{CC} = 15V$, $\beta = 100$, $V_{BE} = 0.6V$

We have $R_C = \frac{V_C - V_{CE}}{I_C} = \frac{15-8}{2\times10^{-3}} = \underline{3.5k\Omega}$ (Load resistance)

& $R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{15-0.6}{0.02\times10^{-3}} = \underline{720k\Omega}$

$\left(I_B = \frac{I_C}{\beta} = \frac{2\times10^{-3}}{100} = 0.02mA\right)$

Fig (9) shows base resistor bias CKt.



(11) A base bias circuit in fig (10) is subjected to an increase in temperature from 25°C to 75°C. If $\beta = 100$ at 25°C & 150 at 75°C, determine the percentage change in Q-Point values over this temperature range. Neglect change in V_{BE} & the effects of leakage current.

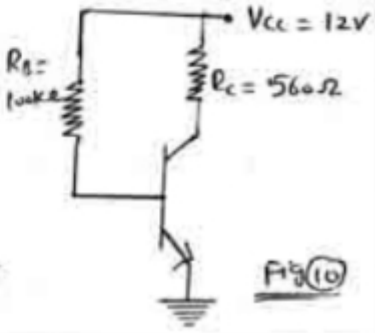


Fig (10)

Sol: At 25°c

$I_B = \frac{V_{cc} - V_{BE}}{R_B} = \frac{12 - 0.7}{100 \times 10^3} = 0.113\,mA$

$I_C = \beta I_B = 100 \times 0.113 \times 10^{-3} = 11.3\,mA$

$V_{CE} = V_{cc} - I_C R_C = 12 - 11.3 \times 10^{-3} \times 560$

$V_{CE} = 5.67V$

At 75°c

$I_B = \frac{12 - 0.7}{100 \times 10^3} = 0.113\,mA$

$I_C = \beta I_B = 150 \times 0.113 \times 10^{-3}$

$I_C = 17\,mA$

$V_{CE} = V_{cc} - I_C R_C$

$= 12 - 17 \times 10^{-3} \times 560$

$= 2.48V$

% age Change in I_C is,

$$\Delta I_C(\%) = \frac{I_C(75°c) - I_C(25°c)}{I_C(25°c)} \times 100$$

$$= \frac{17 \times 10^{-3} - 11.3 \times 10^{-3}}{11.3 \times 10^{-3}} \times 100$$

$= 50\%$ (Increase) (I_C changes by the same percentage as β)

% age change in V_{CE} is,

$$\Delta V_{CE}(\%) = \frac{V_{CE}(75°c) - V_{CE}(25°c)}{V_{CE}(25°c)} \times 100$$

$$= \frac{2.48 - 5.67}{5.67} \times 100$$

$= -56.3\%$ (Decrease)

Comment: Q-Point is extremely dependent on β. Therefore base bias circuit is very unstable

(11) Fig (11) shows the characteristics, determine V_{cc}, R_C & R_B. (Base bias circuit)

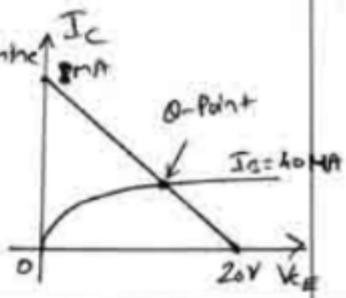


Fig (11)

Sol: From the dc load line (given), $V_{cc} = 20V$

$$I_c = \frac{V_{cc}}{R_c} \quad @ \quad R_c = \frac{V_{cc}}{I_c}$$

$$R_c = \frac{20}{8\times10^{-3}}$$

$$R_c = 2.5K\Omega$$

(Use $R_c = 2.4K\Omega$ Standard Value)

We have, $I_B = \frac{V_{cc} - V_{BE}}{R_B}$

$$\Rightarrow \quad R_B = \frac{20 - 0.7}{40\times10^{-6}}$$

(From the characteristics, $I_B = 40\mu A$)

$$R_B = 482.5K\Omega \text{ (Use } R_B = 470K\Omega \text{ Standard Value)}$$

(12) A base bias circuit has $V_{cc} = 20V$, $R_B = 400K\Omega$, $R_c = 2.2K\Omega$, $V_{CE} = 2V$. Calculate β. Determine the new V_{CE} when a new transistor with $\beta = 100$ is used.

Sol: Given $V_{cc} = 20V$, $R_B = 400K\Omega$, $R_c = 2.2K\Omega$, $V_{CE} = 2V$, $\beta = ?$

We have, $I_c = \frac{V_{cc} - V_{CE}}{R_c} = \frac{20-2}{2.2\times10^{3}} = 8.181mA$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B} = \frac{20-0.7}{400\times10^{3}} = 48.25\mu A$$

Now, $\beta\ (h_{FE}) = \frac{I_c}{I_B} = \frac{8.181\times10^{-3}}{48.25\times10^{-6}} = 169.55$

Now $V_{CE} = ?$, $\beta = 100$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B} = \frac{20-0.7}{400\times10^{3}} = 48.25\mu A$$

$$I_c = h_{FE} I_B = 100 \times 48.25\times10^{-6} = 4.825mA$$

$$V_{CE} = V_{cc} - I_c R_c = 20 - 4.825\times10^{-3}\times 2.2\times10^{3}$$

$$V_{CE} = 9.385V$$

(13) (a) Analyze the voltage-divider bias circuit shown in fig (13) to determine the emitter voltage, collector voltage, & collector-emitter voltage.

(b) Accurately analyze fig (13) to determine I_C, V_E, V_C & V_{CE} when $h_{FE} = 100$

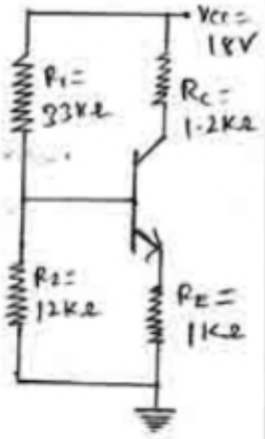


Fig (13)

Sol: (a)

We have $V_B = \frac{V_{cc} R_2}{R_1 + R_2} = \frac{18 \times 12 \times 10^3}{33 \times 10^3 + 12 \times 10^3} = 4.8V$

$V_E = V_B - V_{BE} = 4.8 - 0.7 = 4.1V$

$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{4.8 - 0.7}{1 \times 10^3} = 4.1mA$ // $\quad I_C \simeq I_E = 4.1mA$

$V_C = V_{cc} - I_C R_c = 18 - 4.1 \times 10^{-3} \times 1.2 \times 10^3 = 13.1V$

$V_{CE} = V_C - V_E = 13.1 - 4.1 = 9V$

(b) We have $V_T = \frac{V_{cc} R_2}{R_1 + R_2} = \frac{18 \times 12 \times 10^3}{33 \times 10^3 + 12 \times 10^3} = 4.8V$

$R_T = R_1 \| R_2 = 33 \times 10^3 \| 12 \times 10^3 = 8.8 K\Omega$

$I_B = \frac{V_T - V_{BE}}{R_T + R_E (1 + h_{FE})} = \frac{4.8 - 0.7}{8.8 \times 10^3 + 1 \times 10^3 (1 + 100)} = 37.3MA$

$I_C = h_{FE} I_B = 100 \times 37.3 \times 10^{-6} = 3.73mA$ //

$I_E = I_B + I_C = 37.3 \times 10^{-6} + 3.73 \times 10^{-3} = 3.77mA$ //

$V_E = I_E R_E = 3.77 \times 10^{-3} \times 1 \times 10^3 = 3.77V$ //

$V_C = V_{cc} - I_C R_c = 18 - 3.73 \times 10^{-3} \times 1.2 \times 10^3 = 13.52V$

$V_{CE} = V_C - V_E = 13.52 - 3.77 = 9.75V$

Q-Point is $Q(V_{CE}, I_C) = Q(9.75, 3.73 \times 10^{-3})$

(14) (a) Accurately analyze the Voltage-divider bias circuit shown in fig (14) for $h_{FE(min)} = 50$

(b) Repeat part (a) for $h_{FE(max)} = 200$

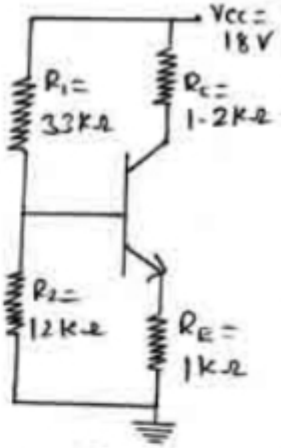


Fig (14)

Ans:

(a) We have $V_T = \frac{V_{cc} R_2}{R_1+R_2} = \frac{18 \times 12\times10^3}{33\times10^3+12\times10^3} = 4.8V$

$R_T = R_1 \| R_2 = \frac{R_1 R_2}{R_1+R_2} = \frac{33\times10^3 \times 12\times10^3}{33\times10^3+12\times10^3} = 8.8K\Omega$

$I_B = \frac{V_T - V_{BE}}{R_T + R_E(1+h_{FE})} = \frac{4.8-0.7}{8.8\times10^3 + 1\times10^3(1+50)} = 68.6\mu A$

$I_C = h_{FE} I_B = 50 \times 68.6\times10^{-6} = 3.43mA$

$I_E = I_B + I_C = 68.6\times10^{-6} + 3.43\times10^{-3} = 3.5mA$

$V_E = I_E R_E = 3.5\times10^{-3} \times 1\times10^3 = 3.5V$

$V_C = V_{cc} - I_C R_C = 18 - 3.43\times10^{-3} \times 1.2\times10^3 = 13.9V$

$V_{CE} = V_C - V_E = 12.9 - 3.5 = 10.4V$

Q-Point $Q(V_{CE}, I_C) = Q(10.4, 3.43\times10^{-3})$

(b) We have, $V_T = 4.8V$, $R_T = 8.8K\Omega$

$I_B = \frac{V_T - V_{BE}}{R_T + R_E(1+h_{FE})} = \frac{4.8-0.7}{8.8\times10^3 + 1K(1+200)} = 19.5\mu A$

$I_C = h_{FE} I_B = 200 \times 19.5\times10^{-6} = 3.9mA$

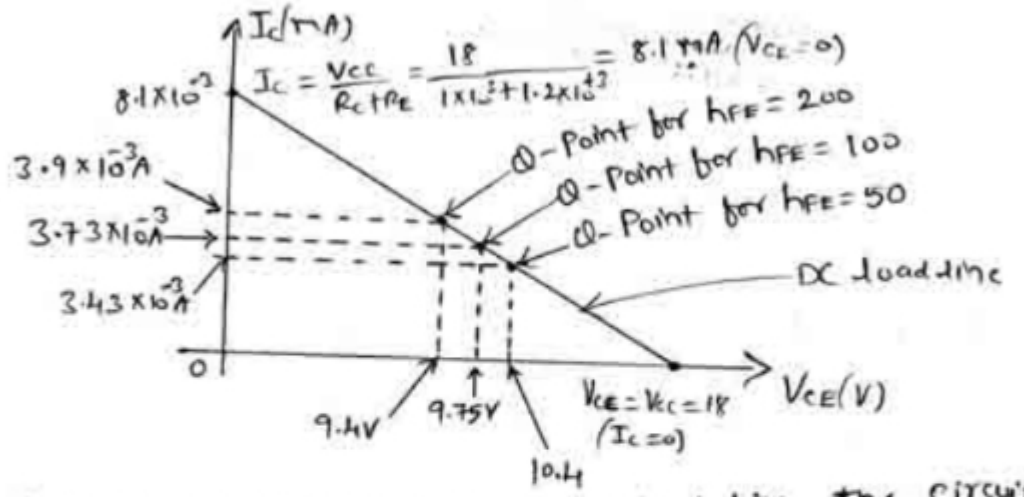
$I_E = I_B + I_C = 19.5\times10^{-6} + 3.9\times10^{-3} = 3.92\text{ mA}$

$V_E = I_E R_E = 3.92\times10^{-3}\times 1\times10^{3} = 3.92\text{ V}$

$V_C = V_{CC} - I_C R_C = 18 - 3.9\times10^{-3}\times 1.2\times10^{3} = 13.3\text{ V}$

$V_{CE} = V_C - V_E = 12.3 - 3.92 = 9.4\text{ V}$

Q-Point, $Q(V_{CE}, I_C) = Q(9.4, 3.9\times10^{-3})$



Conclusion: • From the above characteristics, the circuit (Voltage divider bias) is insensitive to the change in β.

(a) Q-Point is most insensitive to changes in β.

∴ Voltage-divider bias circuit is most stable bias circuit

(15) For the fig (15), draw the dc load line & determine the operating Point. Assume Si transistor

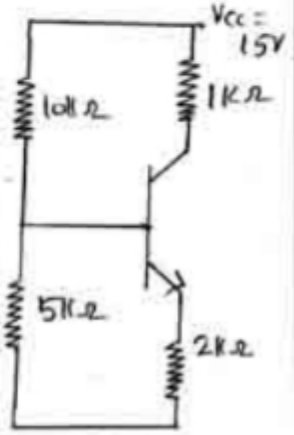
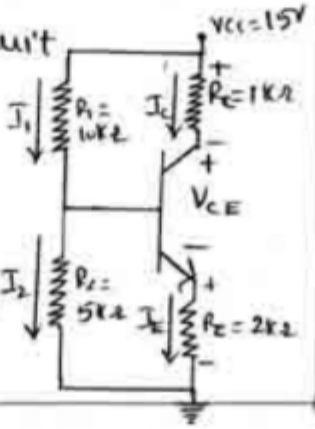


Fig (15)

Sol: DC load line

Redraw the given circuit



Applying KVL to collector-emitter loop,

$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

$\Rightarrow V_{CC} - V_{CE} - I_C(R_C+R_E) = 0$ —(1)

($\because I_E \simeq I_C$)

① Put $I_C = 0$ in ①

$V_{CE} = V_{cc} = 15V$

Mark as Point $A(V_{CE}, I_C) = A(15, 0)$

② Put $V_{CE} = 0$ in ①

$$I_C = \frac{V_{cc}}{R_C + R_E} = \frac{15}{1\times10^3 + 2\times10^3} = 5mA$$

Mark as Point $B(V_{CE}, I_C) = B(0, 5\times10^{-3})$

Draw a straight through $A(15,0)$ & $B(0, 5\times10^{-3})$ to get dc load line as shown in fig 15(a)

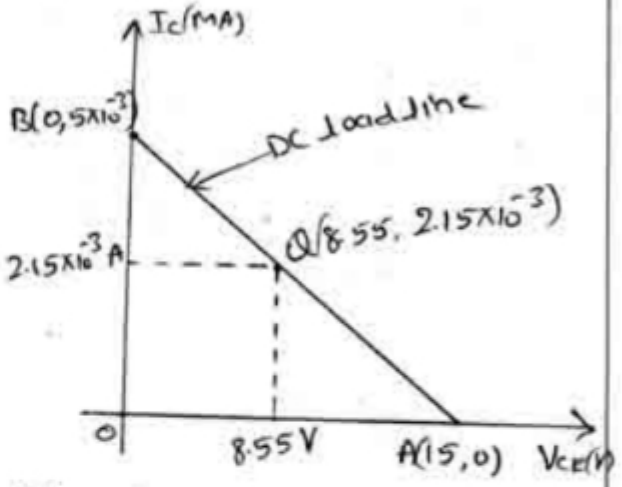
Operating Point (Q-Point)

Volt across R_2,

$$V_B = \frac{V_{cc}\ R_2}{R_1 + R_2}$$

$$= \frac{15 \times 5\times10^3}{10\times10^3 + 5\times10^3}$$

$V_B = 5V$



Emitter current,

$$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{5 - 0.7}{2\times10^3} = 2.15mA$$

Collector current,

$$(I_{CQ} =)\ I_C \simeq I_E = 2.15mA$$

Collector-emitter Voltage,

$$(V_{CEQ} =) V_{CE} = V_{cc} - I_C(R_C + R_E)$$

$$= 15 - 2.15\times10^{-3}(1\times10^3 + 2\times10^3)$$

$$= 8.55V$$

$\therefore$ Q-Point is $Q(V_{CEQ}, I_{CQ}) = Q(8.55, 2.15\times10^{-3})$

Mark operating Point at $Q(8.55, 2.15\times10^{-3})$

6) A Potential divider bias circuit has $R_1 = 50k\Omega$, $R_2 = 10k\Omega$ & $R_E = 1k\Omega$. If $V_{cc} = 12V$, find ⓓ Stability factor. ($\beta = 100$)

ⓐ the value of I_C, given $V_{BE} = 0.1V$. ⓔ Saturation current ($R_C = 1.2k\Omega$)

ⓑ I_C, given $V_{BE} = 0.3V$ ⓒ Comment on the result.

4: Given $R_1 = 50\times10^3\,\Omega$, $R_2 = 10\times10^3\,\Omega$, $R_E = 1\times10^3\,\Omega$; $V_{cc} = 12V$

(a) $V_B = \frac{V_{cc}\,R_2}{R_1+R_2} = \frac{12 \times 10\times10^3}{50\times10^3 + 10\times10^3} = 2V$

Collector current, $I_c = \frac{V_B - V_{BE}}{R_E} = \frac{2-0.1}{1\times10^3} = 1.9mA$

(b) $V_B = 2V$

$I_c = \frac{V_B - V_{BE}}{R_E} = \frac{2-0.3}{1\times10^3} = 1.7mA$

(c) V_{BE} varies by 200%, the value of I_c changes by nearly 10%. ∴ In voltage-divider bias circuit, I_c is almost independent of transistor parameter variations.

(d) $S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E+R_{TH}}\right)} = \frac{1+100}{1+100\left(\frac{1\times10^3}{1\times10^3+8.33\times10^3}\right)}$

$S = 8.6$

$R_{TH} = \frac{R_1 R_2}{R_1+R_2} = \frac{50\times10\,10^6}{(50+10)10^3}$

$R_{TH} = 8.33k\Omega$

(e) $I_{C(sat)} = \frac{V_{cc}}{R_{TH}+R_E} = \frac{12}{1.2\times10^3+1\times10^3} = 5.45mA$

(7) (a) Determine the dc bias voltage V_{CE} & the current I_c for the voltage-divider circuit of fig (17)

(b) Repeat the analysis of fig (17) using the approximate technique & compare solutions for I_{CQ} & V_{CEQ}.

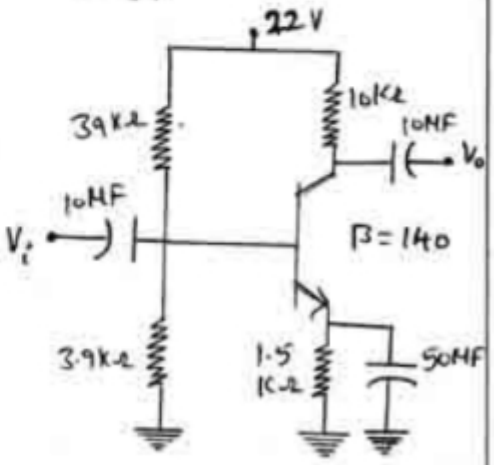


Fig (17)

(or:

(a) $V_T = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{22(3.9\times10^3)}{39\times10^3 + 3.9\times10^3} = 2V$

$R_T = \frac{R_1 R_2}{R_1 + R_2} = \frac{39\times10^3 \times 3.9\times10^3}{39\times10^3 + 3.9\times10^3} = 3.55K\Omega$

$I_B = \frac{V_T - V_{BE}}{R_T + R_E(1+h_{FE})} = \frac{2 - 0.7}{3.55\times10^3 + 1.5\times10^3(141)} = 6.05MA$

$I_C = h_{FE} I_B = 140 \times 6.05\times10^{-6} = 0.85MA$ $(I_E = I_B + I_C = 0.85mA = I_C)$

$V_{CE} = V_{CC} - I_C(R_C + R_E) = 22 - 0.85\times10^{-3}(10\times10^3 + 1.5\times10^3)$

$V_{CE} = 12.22V$

(b) $V_B = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{22 \times 3.9\times10^3}{39\times10^3 + 3.9\times10^3} = 2V$

$V_E = V_B - V_{BE} = 2 - 0.7 = 1.3V$

$(I_{CQ} =)\ I_C \simeq I_E = \frac{V_B - V_{BE}}{R_E} = \frac{1.3}{1.5\times10^{+3}} = 0.867mA$

$(V_{CEQ} =)\ V_{CE} = V_{CC} - I_C(R_C + R_E) = 22 - 0.867\times10^{-3}(10K + 1.5K)$

$(V_{CEQ})\ V_{CE} = 12.03V$

Comparision:

Analysis	$I_{CQ}(I_C)$	$V_{CEQ}(V_{CE})$
Exact	0.85mA	12.22V
Approximate	0.867mA	12.03V

The values of I_{CQ} & V_{CEQ} are very close. (The larger the level of R_1 compared to R_2, the closer the approximate to the exact solution).

(8) Design a base bias circuit to have $V_{CE} = 5V$ & $I_C = 5mA$. The supply voltage is 15V, $h_{FE} = 100$

Sol: $R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{15-5}{5\times10^{-3}} = 2k\Omega$ //..

(Use $1.8k\Omega$ @ $2.2k\Omega$ Standard Value)

$I_B = \frac{I_C}{h_{FE}} = \frac{5\times10^{-3}}{100} = 50\mu A$

$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{15-0.7}{50\times10^{-6}} = 286k\Omega$ //..

(Use $270k\Omega$ @ $330k\Omega$ Standard Value)

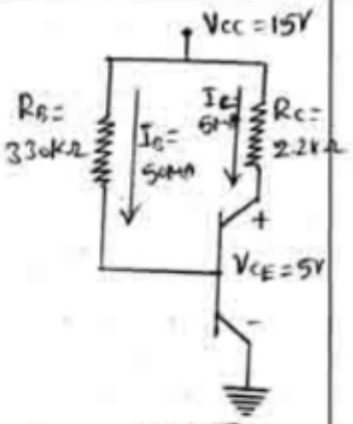


Fig (18)

The base bias circuit is shown in fig (18)

(9) Given $I_{CQ} = 2mA$ & $V_{CEQ} = 10V$. determine R_1 & R_C of Potential divider circuit shown in fig (19)

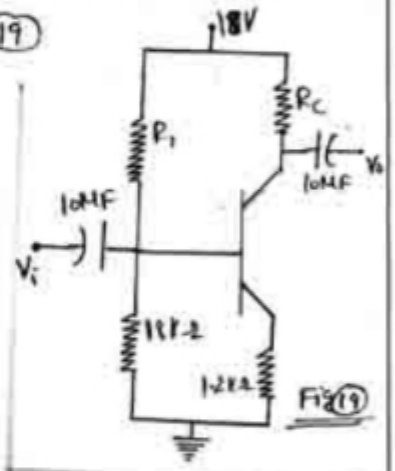


Fig (19)

Sol: $V_E = I_E R_E = 2\times10^{-3} \times 1.2\times10^{3} = 2.4V$

$(\because I_C \simeq I_E)$

$V_B = V_{BE} + V_E = 0.7 + 2.4 = 3.1V$

$V_B = \frac{V_{CC} R_2}{R_1 + R_2}$

$\Rightarrow 3.1 = \frac{18 \times 18\times10^{3}}{R_1 + 18\times10^{3}}$

$\Rightarrow$ $\boxed{R_1 = 86.52k\Omega}$ (Use $82k\Omega$ @ $91k\Omega$ Standard Value) //..

$V_C = V_{CE} + V_E = 10 + 2.4 = 12.4V$

$R_C = \frac{V_{CC} - V_{CE}}{I_C} - R_E$ (or) $\frac{V_{CC} - V_C}{I_C}$

$= \frac{18-10}{2\times10^{-3}} - 1.2\times10^{+3}$

$\boxed{R_C = 2.8k\Omega}$ //..

(5) Design the voltage divider bias circuit to have $V_{CE} = V_E = 5V$ & $I_C = 5mA$ When the supply voltage is 15V. Assume $h_{FE} = 100$.

Given $V_{CE} = 5V$, $V_E = 5V$, $I_C = 5mA$, $h_{FE} = 100$. $V_{CC} = 15V$

Assume $V_{BE} = 0.7V$.

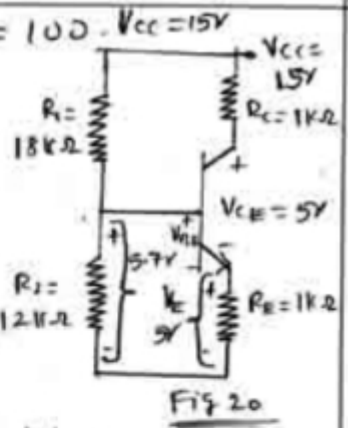


Fig 20

Step 1: Let $I_2 = \frac{I_C}{10} = \frac{5\times10^{-3}}{10} = 500\mu A$

Step 2: $R_E = \frac{V_E}{I_C} = \frac{5}{5\times10^{-3}} = 1k\Omega$

Step 3: $R_2 = \frac{V_B}{I_2} = \frac{V_{BE}+V_E}{I_2} = \frac{0.7+5}{500\times10^{-6}} = 11.4k\Omega$

(Use 12kΩ Standard Value)

Step 4: $R_1 = \frac{V_{CC}-V_B}{I_2} = \frac{15-(V_{BE}+V_E)}{500\times10^{-6}} = \frac{15-0.7-5}{500\times10^{-6}} = 18.6k\Omega$

(Use 18kΩ Standard Value)

Step 5: $R_C = \frac{V_{CC}-V_{CE}-V_E}{I_C} = \frac{15-5-5}{5\times10^{-3}} = 1k\Omega$

The Voltage divider bias circuit is shown in fig (20)

(21) Design the voltage-divider bias circuit to operate from a 12V supply. Given $V_{CE} = 3V$, $V_E = 5V$ & $I_C = 1mA$.

Sol: Given $V_{CC} = 12V$, $V_{CE} = 3V$, $V_E = 5V$, $I_C = 1mA$.

Assume $V_{BE} = 0.7V$.

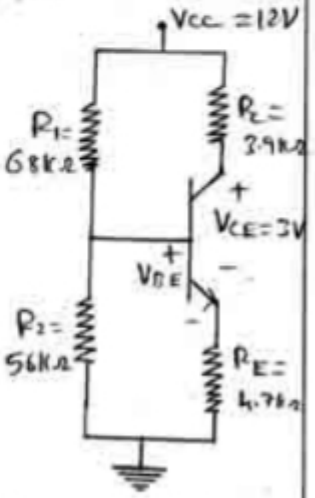


Fig (21)

Step 1: $I_2 = \frac{I_C}{10} = \frac{1\times10^{-3}}{10} = 100\mu A$

Step 2: $R_E = \frac{V_E}{I_C} = \frac{5}{1\times10^{-3}} = 5k\Omega$ (Use 4.7kΩ Standard Value)

Step 3: $R_2 = \frac{V_B}{I_2} = \frac{V_{BE}+V_E}{I_2} = \frac{0.7+5}{100\times10^{-6}}$ (or) $\frac{0.7+4.7}{100\times10^{-6}}$

$R_2 = 57k\Omega$ (or) $54k\Omega$ (If $R_E = 4.7k\Omega$)

(Use 56kΩ Standard Value)

Step 4: $R_1 = \frac{V_{CC}-V_B}{I_2} = \frac{V_{CC}-V_{BE}-V_E}{I_2} = \frac{12-0.7-5}{100\times10^{-6}}$ (or) $\frac{12-0.7-4.7}{96.4\times10^{-6}}$

$R_1 = 63\,k\Omega$ @ $68.46\,k\Omega$

If $R_E = 4.7k\Omega$

$\Rightarrow V_E = R_E I_C$

$= 4.7\times10^{3}\times10^{-3}$

$\boxed{V_E = 4.7V}$

$\Rightarrow I_2 = \frac{V_B}{R_2}$

$= \frac{5.4}{56\times10^{3}}$

$\boxed{I_2 = 96.4\mu A}$

Step 5: $R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C}$

$= \frac{12-3-5}{1\times10^{-3}}$ @ $\frac{12-3-4.7}{1\times10^{-3}}$

$R_C = 4k\Omega$ @ $4.3k\Omega$

(Use $3.9k\Omega$ standard value)

The Voltage-divider circuit is shown in fig (21)

(12) Determine V_{CE} for the Voltage-divider bias Configuration of fig (22)

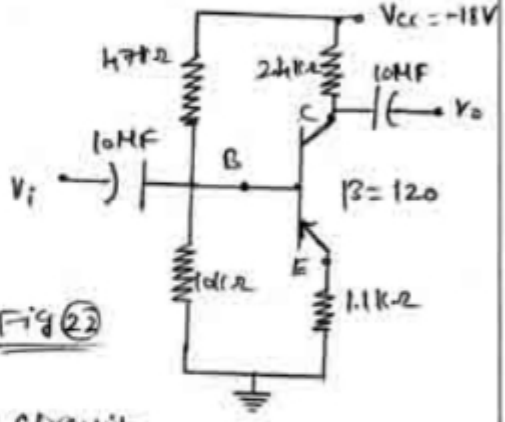
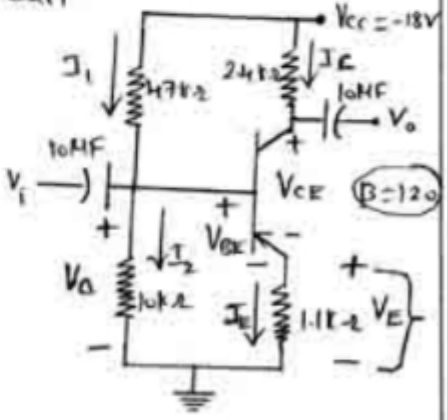


Fig (22)

Sol: The given Voltage-divider bias circuit is shown in fig 22@



$V_B = \frac{-V_{CC}\,R_2}{R_1+R_2}$ $\left[-V_{CC} - I_1R_1 - I_2R_2 = 0 \;\Rightarrow\; I_2 = -\frac{V_{CC}}{R_1+R_2}\left(I_1 \simeq I_2\right),\; V_B = \left(\frac{-V_{CC}}{R_1+R_2}\right)R_2\right]$

$= \frac{-18\times10k}{47k+10k}$

$= -3.16V$

$V_E = V_B - V_{BE}$ $[\because V_B = V_{BE} + V_E]$

$= -3.16 - (-0.7)$ $(V_{BE} = -0.7V$ for PNP transistor with a bare circuit)

$= -2.46V$

$$I_E = \frac{V_E}{R_E} = \frac{-2.46}{1.1\times10^3} = -2.24\text{mA}$$

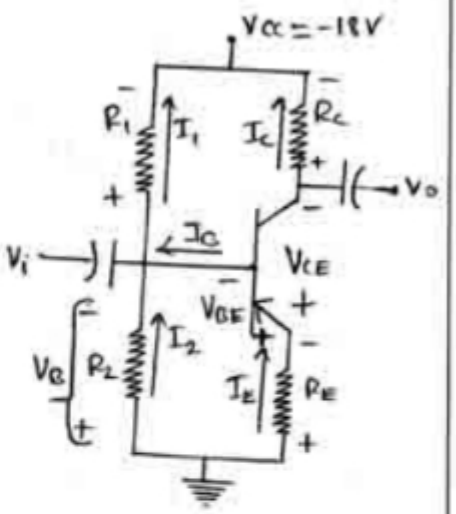
$$I_C \simeq I_E = -2.24\text{mA}$$

$$V_{CE} = -V_{CC} - I_C(R_C + R_E) \quad [-V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0]$$

$$= -18 - (-2.24\times10^{-3})(2.4\text{K} + 1.1\text{K})$$

$$= -10.16\text{V}$$

(OR) The given voltage-divider bias



$$I_2 = \frac{V_{CC}}{R_1+R_2} = \frac{18}{47\text{K}+10\text{K}} = 0.316\text{mA}$$

$$\left(\because -V_{CC} + I_1R_1 + I_2R_2 = 0,\ I_1 \simeq I_2\right)$$

$$V_B = I_2R_2 = 3.16\text{V}$$

$$V_E = V_B - V_{BE} = 3.16 - 0.7 = 2.46\text{V}$$

$$I_E = \frac{V_E}{R_E} = \frac{2.46}{1.1\times10^3} = 2.24\text{mA}$$

$$I_C \simeq I_E = 2.24\text{mA}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 18 - 2.24\times10^{-3}(2.4\text{K} + 1.1\text{K})$$

$$= 10.16\text{V}$$

Syllabus: Ideal OPAMP, Inverting and Non-inverting OP-AMP circuits, OP-AMP applications: Voltage follower, addition, subtraction, integration, differentiation, Numerical examples as applicable.

* Operational amplifier (or) op-amp:

An OP-amp is a very high gain differential amplifier with high input impedance and low output impedance.

(or)

An OP-amp is a direct-coupled high-gain amplifier usually consisting of one (or) more differential amplifiers and usually followed by a level translator and an output stage.

Note:

① An OP-amp is a linear integrated circuit (IC)

② The OP-amp is a versatile device (Used to amplify both AC and dc input signals)

③ OP-amp is used to perform mathematical operations such as addition, subtraction, differentiation and integration.

④ Robert J. Widlar invented MA 741 IC (An internally compensated op-amp) in 1968

MA → Fairchild (Manufacturer)

⑤ Advantages of OP-AMP over transistor amplifier

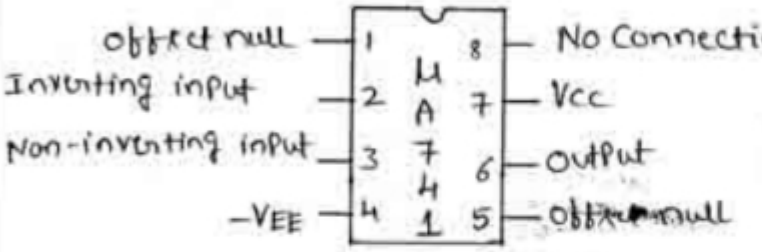
- Less power consumption
- Low cost
- More compact
- More reliable
- Easy design
- Versatile device
- Higher gain can be obtained

etc

⑥ Applications of op-amp.

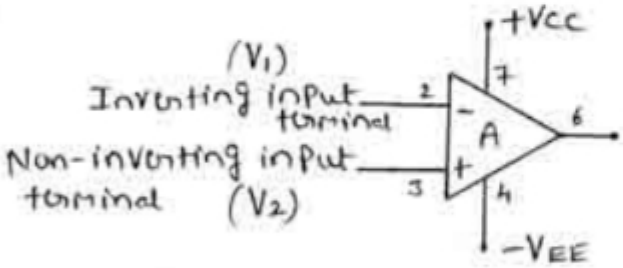
- AC and dc signal amplification
- Active filters.
- Oscillators
- Comparators
- Regulators
- Biomedical instrumentation. etc

⑦ Pin diagram of OP-amp (MA 741 IC)



Fig①: Pin diagram of op-amp

⑧ Circuit Symbol of OP-amp ⑥ Schematic Symbol



Fig②: Circuit Symbol of op-amp

⑨ ⓐ Single-Ended input: Input signal is connected to one input with the other input connected to ground.

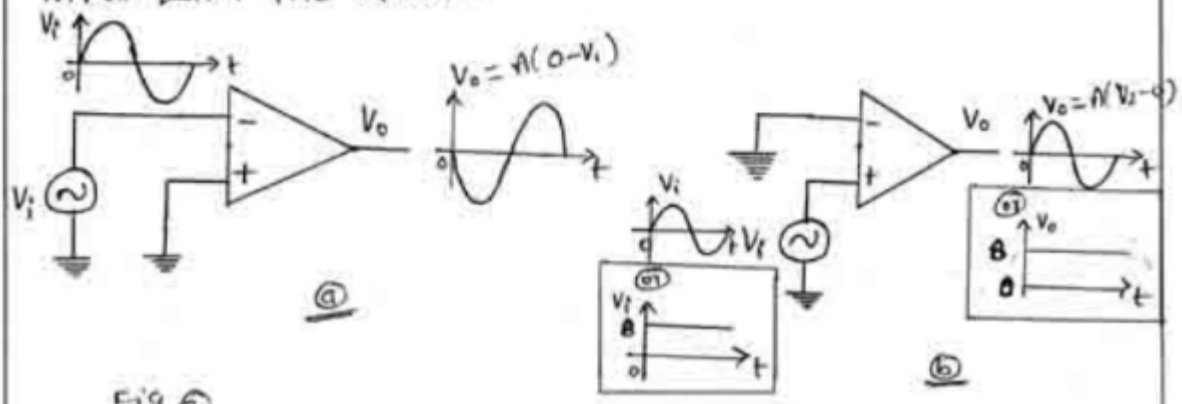
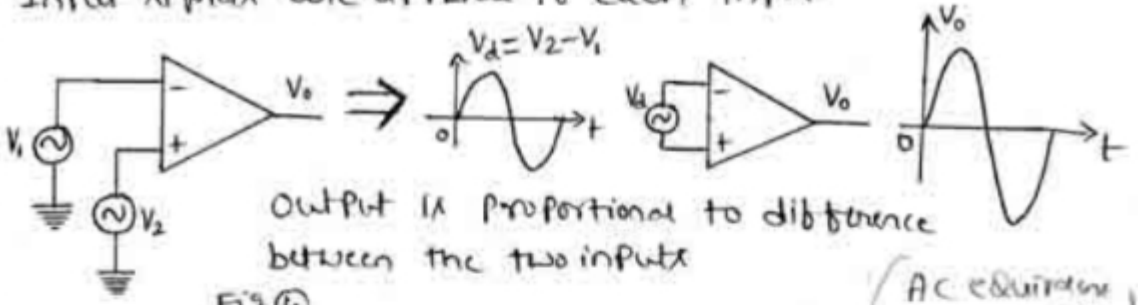


Fig ⑤

(b) Double-Ended (Differential) Input :

Input signals are applied to each input



Output is proportional to difference between the two inputs

Fig (4)

(AC equivalent ckt)

(a) Equivalent circuit (b) Circuit model of op-amp :

Fig (5) shows the simplified circuit model of practical op-amp.

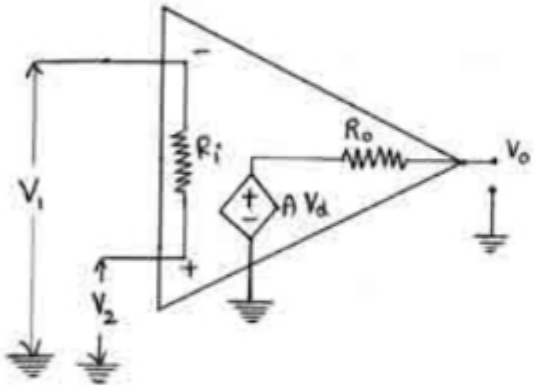


Fig (5) : circuit model of practical op-amp

→ AV_d $[A(V_2 - V_1)]$ is the Thevenin equivalent voltage source & R_o is the Thevenin equivalent resistance

→ A is the gain & Large signal voltage gain

→ R_i is the input resistance

→ V_d $(V_2 - V_1)$ is the difference input voltage.

Fig (6) shows the Equivalent circuit of ideal op-amp.

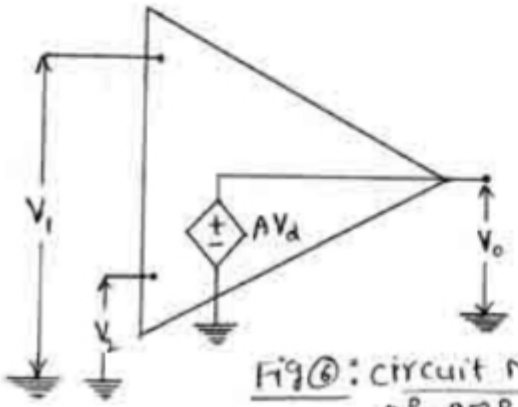


Fig (6) : circuit model of ideal op-amp

→ An ideal op-amp has $A = \infty$, $R_i = \infty$ & $R_o = 0$

(11) Package types

There are three basic types of Linear Ic packages:
(a) The flat pack (b) The metal can (c) transistor pack
(d) The dual-in-line package (DIP)

(12) Features of 741

- No external frequency compensation required
- Short-circuit protection.
- Offset null capability
- Large common-mode and differential voltage ranges.
- Low power consumption.
- No Latch-up problem.

(13) Differential amplifier:

It amplifies the difference of the two inputs $V_d (V_2 - V_1)$

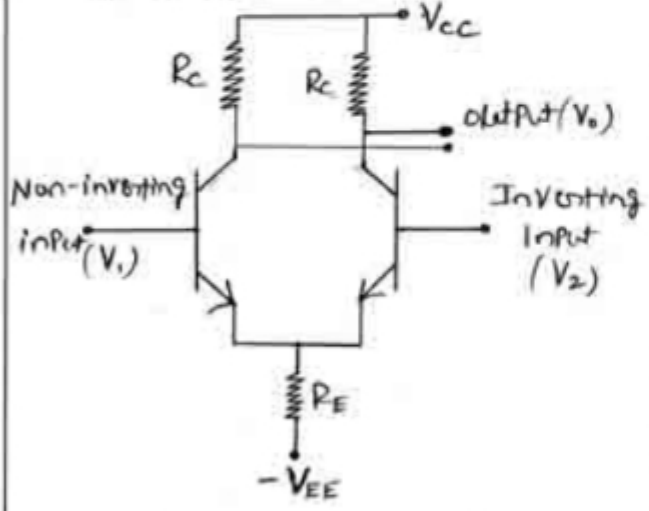


Fig (4): Differential amplifier

Output is,

$V_o \propto (V_1 - V_2)$

$\Rightarrow \boxed{V_o = A(V_1 - V_2)}$ (or)

$\boxed{V_o = A V_d}$

Where,

A → Large signal voltage gain
V_1 → voltage applied to the non-inverting input
V_2 → voltage applied to inverting input
V_d → difference voltage

(14) • OP-amps which use BJT are called bipolar type opamp
• OP-amps having FET input circuit with the remainder of the circuit using BJT are called FET type OP-amps

* **Block diagram of OP-amp (or) Internal Block diagram (or) Architecture of op-amp:**

The block diagram of an OP-amp is shown in fig (8)

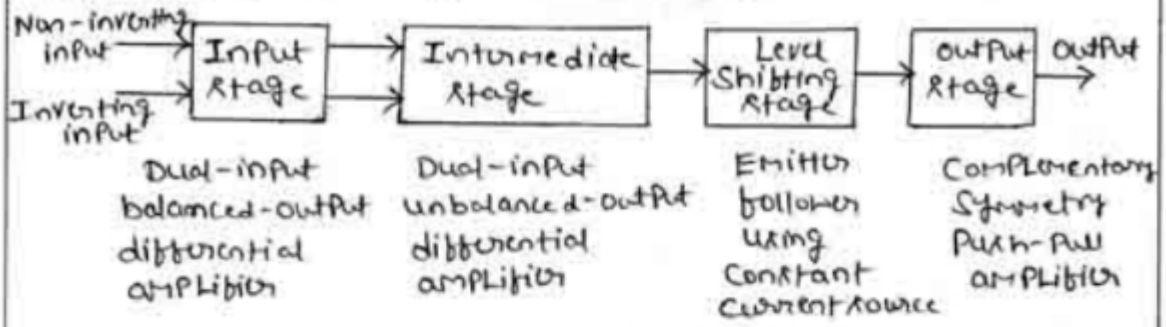


Fig (8): Block diagram of a typical op-amp

There are four stages:

① **Input Stage (or) Differential amplifier stage**

- It can amplify difference between the two input signals.
- Input resistance is very high, draws zero current from the input sources.

② **Intermediate stage (Stages) (or) High gain amplifier stage**

- It uses direct coupling.
- It provides very high gain.

③ **Level translator stage (or) Level shifter stage (Buffer)**

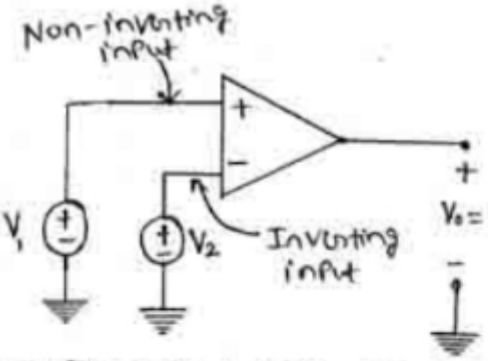
- It shifts the dc level of the output voltage of the intermediate stage to zero.

④ **output Stage (or) Power amplifier stage (or) driver stage**

- It has very small output resistance.
- output voltage is the same irrespective of the value of the load resistance connected to the output terminal.

Note: (I) Configurations (or) Voltage gain of OP-amp:

① Open-loop Configuration ② Open-loop Voltage gain (A_{OL})



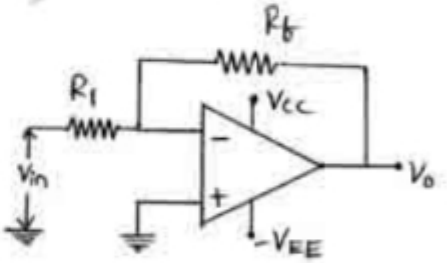
Fig①: Open loop Configuration

- A_{OL} is the open-loop voltage gain of op-amp (Typically $A_{OL} = 2 \times 10^5$)
- A_{OL} is the maximum possible voltage gain.
- There is no feedback from the output to input

- If input is in micro volts, output will be in volts.
- Output voltage cannot cross the value of power supply (③ Saturation Value) V_{cc} (or V_{EE})
- So, if input is in milli volts, output reaches saturation value $V_{sat} = V_{cc}$ (or V_{EE}). This property of op-amp is called Saturation Property.

② Closed-loop Configuration ③ Closed-loop Voltage gain (A_{CL})

- Open-loop voltage gain of op-amp is very high. Such high gain is not required in most applications.
- In order to reduce gain, Negative feedback is used (a part of the output signal is fed back in phase opposition to the input)



Fig④: Negative feedback op-amp circuit (Closed loop Configuration)

- Many other op-amp characteristics are improved with this.

③ Total output of a differential amplifier (practically) ④ (Op-amp)

The output of op-amp (DA) is. (DA → Differential Amplifier)

$$V_o = A_d V_d \quad - (1)$$

Where, A_d → Differential gain (Gain with which the DA amplifies the difference between two input signals)

$$A_d = \frac{V_o}{V_d}$$

V_d → Difference between two inputs $(V_1 - V_2)$

If $V_1 = V_2$, then ideally output is zero. $(V_o = 0)$

But in practical op-amp. output is,

$$V_o = A_{cm} V_{cm} \quad - (2)$$

$$A_{cm} = \frac{V_o}{V_{cm}}$$

Where A_{cm} → Common mode gain (Gain with which DA amplifies the common mode signal)

V_{cm} → Common mode signal $\left(\frac{V_1 + V_2}{2}\right)$

∴ Total output is,

$$V_o = A_d V_d + A_{cm} V_{cm}$$

$$\boxed{V_o = A_d V_d \left(1 + \frac{1}{CMRR} \frac{V_{cm}}{V_d}\right)} \quad \left[\because CMRR = \frac{A_d}{A_{cm}}\right]$$

(iii) $A_d\,(dB) = 20 \log_{10}(A_d)$

Op-amp parameters & Characteristics

(1) Differential gain (or) Differential Mode gain (A_d) (or) Large signal voltage gain (A)

It is the factor by which the difference between the two input signals is amplified by the op-amp.

(or)

It is the ratio of the output voltage to the difference voltage. It is denoted by A_d

ie $A_d = \frac{V_o}{V_d} = \frac{V_o}{V_1 - V_2}$

Ideally: $A_d = \infty$
Practically: $A_d = A = 2 \times 10^5$ (HA741)

② Common mode gain (A_{cm})

It is the factor by which the common mode input voltage is amplified by the op-amp.

It is the ratio of the output voltage to the common mode signal. It is denoted by 'A_{cm}'

ie $A_{cm} = \frac{V_o}{V_{cm}} = \frac{V_o}{(V_1 + V_2)/2}$

Ideally: $A_{cm} = 0$
Practically: $A_{cm} = 6 - 7$ (HA741)

③ Common mode rejection ratio (CMRR)

It is the factor which explains the ability of an op-amp to reject the common mode signal.

It is the ratio of differential gain to common mode gain. It is denoted by 'CMRR'.

ie $CMRR = \frac{A_d}{A_{cm}}$ or $CMRR(dB) = 20 \log_{10}\left(\frac{A_d}{A_{cm}}\right)(dB)$

Ideally: CMRR = ∞
Practically: CMRR = 90dB (HA741)

(Ad is known as large-signal voltage gain A)

④ Differential input resistance or Input resistance or Input impedance (R_i)

It is the equivalent resistance measured at either the inverting or non-inverting input terminal with the other terminal connected to ground. It is denoted by 'R_i'

Ideally: $R_i = \infty$
Practically: $R_i = 2M\Omega$ (For HA741)

⑤ Output resistance or Output impedance (R_o)

It is the equivalent resistance measured between the output terminal of the OP-amp and the ground. It is denoted by R_o.

Ideally: $R_o = 0$
Practically: $R_o = 75\Omega$ (MA 741)

⑥ Bandwidth (BW)

It is the range of frequency over which the gain of OP-amp is almost constant.

It is the range of frequency over which the performance of the OP-amp is satisfactory. It is denoted by BW.

μA741IC is more or 741C

Ideally: BW = ∞
Practically: BW = 1MHz (741C)

⑦ Input offset voltage (V_{io})

It is the voltage that must be applied between the two input terminals of an OP-amp to make output voltage zero (to null the output). It is denoted by V_{io}.

Ideally: $V_{io} = 0$
practically: $V_{io} = 6mV$ (741C)

$V_{io} = V_1 - V_2$ for $V_o = 0$

⑧ Output offset voltage (V_{oo})

It is the output voltage when both input voltages are zero. It is denoted by V_{oo}.

Ideally: $V_{oo} = 0$
Practically: $V_{oo} = 1mV$ (741C)

⑨ Input offset current (I_{io})

It is the difference between the currents in the input terminals. It is denoted by I_{io}.

ie $I_{io} = |I_1 - I_2|$

Where, I_1 → current into the noninverting input
I_2 → current into the inverting input.

Ideally: $I_{io} = 0$
Practically: $I_{io} = 20nA$ (For HA 7741)

200nA max

(10) Input bias current (I_{ib})

It is the average of the currents in the input terminals. It is denoted by I_{ib}

ie $I_{ib} = \frac{I_1 + I_2}{2}$

Where, I_1, I_2 → current into non-inverting & inverting input respectively.

Ideally: $I_{ib} = 0$
Practically: $I_{ib} = 80nA$ (For HA 7741)

500 nA max

(11) Slew rate (SR)

It is the maximum rate of change of output voltage with respect to time. It is denoted by SR.

ie $SR = \left.\frac{dV_o}{dt}\right|_{max}$ (V/μs)

Ideally: $SR = \infty$
Practically: $SR = 0.5V/\mu s$

(12) Supply voltage rejection ratio or Power supply sensitivity or Power supply rejection ratio: (SVRR) or (PSRR)

It is the change in input offset voltage (V_{io}), caused by variations in supply voltage. It is denoted

by SVRR (or) PSRR.

ie $SVRR = \frac{\Delta V_{io}}{\Delta V}$ $(\mu V/V)$

Ideally: SVRR = 0

Practically: SVRR = 150 μV/V (741C)

Note:

① Input Capacitance (C_i):

It is the equivalent capacitance measured at either the inverting (or) noninverting terminal with the other terminal connected to ground. It is defined by 'C_i'.

Practically: C_i = 1.4PF for 741C

② Gain-Bandwidth product (GB)

It is the bandwidth of the OP-amp when the voltage gain is 1

Practically: GB = 1MHz for 741C

③ Maximum signal frequency interms of Slew rate (for an undistorted output)

Let the output voltage (Sinusoidal signal) be.

$$V_o = V_m \sin(\omega t) \quad — ①$$

Diff w.r.t 't' on b.s

$$\frac{dV_o}{dt} = V_m \cos(\omega t).\omega$$

$$\Rightarrow \left.\frac{dV_o}{dt}\right|_{max} = \omega V_m \quad — ② \qquad (\because \cos(\omega t)|_{max} = 1)$$

To prevent distortion at the output, the rate of change of output w.r.t must be less than the SR.

i.e $\left.\frac{dV_o}{dt}\right|_{max} \leq SR$ — ③

Using ② in ③, we get,

$\omega V_M \leq SR$

$\Rightarrow \omega \leq \frac{SR}{V_M} \Rightarrow$ $\boxed{\omega_{max} = \frac{SR}{V_M}}$ (rad/s)

$\Rightarrow f \leq \frac{SR}{2\pi V_M}$ (∵ $\omega = 2\pi f$) $\Rightarrow$ $\boxed{f_{max} = \frac{SR}{2\pi V_M}}$ (Hz)

④ OP-amp Characteristics:

Sl No	Parameter	Symbol	Ideal Value	Typical value for MA741
1	Differential gain (or) Large signal Voltage gain (or) Open-loop Voltage gain.	A_d (or) A	∞	2×10^5
2	Common mode gain	A_{cm}	0	6
3	Common mode rejection ratio	CMRR	∞	90dB
4	Input resistance	R_i	∞	$2M\Omega$
5	output resistance	R_o	0	75Ω
6	Bandwidth	BW	∞	1MHz
7	Input offset voltage	V_{io}	0	6mV
8	output offset voltage	V_{oo}	0	1mV
9	Input offset current	I_{io}	0	20nA
10	Input bias current	I_{ib}	0	80nA
11	Slew rate	SR	∞	0.5V/μs
12	Supply Voltage rejection ratio	SVRR	0	150μV/V

⑤ Virtual ground (or) Virtual short :

The OP-amp inverting amplifier is shown in fig ⑪

The output voltage is,

$$V_o = A(V_2 - V_1) \quad \text{— (1)}$$

Where, A → Large signal voltage gain

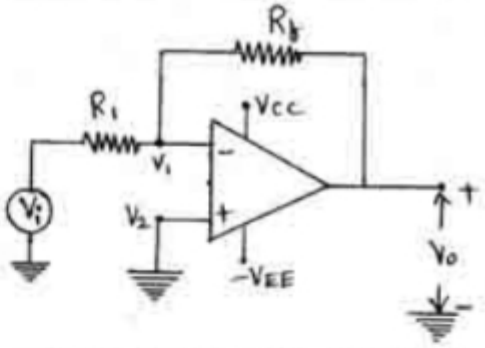


Fig (11): Basic op-amp circuit

For an output voltage of 12V, the input voltage would be,

$$V_2 - V_1 = \frac{V_o}{A} \quad (\because \text{From 1})$$

$$\Rightarrow V_2 - V_1 = \frac{12}{2\times10^5} \quad (\because \text{Practically, } A = 2\times10^5 \text{ for MA741})$$

$$\Rightarrow V_2 - V_1 = 0.06\,mV$$

Differential input voltage is very small. ($V_d = V_2 - V_1$)

Ideally, $V_2 - V_1 = 0$

$$\Rightarrow \boxed{V_1 = V_2} \quad \text{— (2)}$$

From (2), we can conclude,

- Voltage at inverting terminal = Voltage at non-inverting terminal
- There exists a virtual short-circuit or virtual ground
- No current flows through the short circuit
- Current through R_1 = Current through R_f.

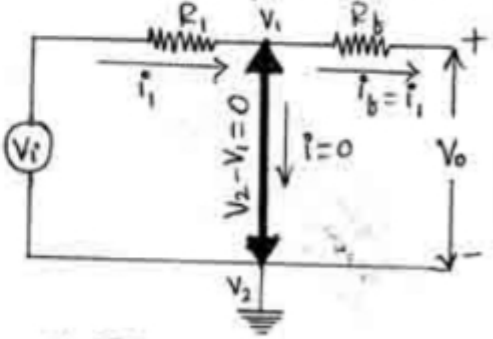


Fig (12): Virtual ground

(6) The virtual short is indicated by a thick line between input terminals.

(7) For an op-amp, output voltage cannot cross V_{cc} (V_{EE}) ($\simeq$ 12 to 15V) (∵ From Saturation Property)

⑧ No current flows into OP-amp input terminals (∵ Input impedance is very high)

---

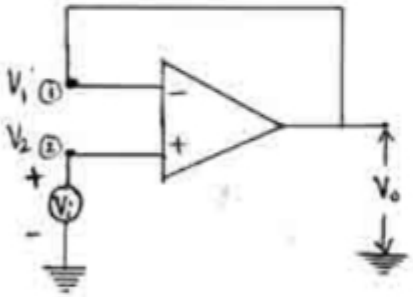
* OP-amp applications

① Voltage follower
② Inverting amplifier
③ Non-inverting amplifier
④ Summer (Adder)
⑤ Subtractor (difference amplifier)
⑥ Differentiator
⑦ Integrator.
⑧ Isolation amplifier ⑨ Source follower
⑩ Unity gain amplifier ⑪ Buffer:

* ① Voltage follower

Definition: An OP-amp circuit in which the output voltage follows the input voltage is called Voltage follower (Output voltage is equal to input voltage)

Circuit diagram:



Analysis:

From Virtual ground concept,

$$V_1 = V_2 = V_i \quad -①$$

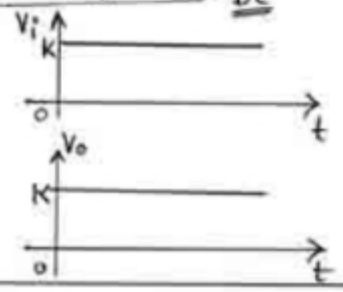
Since output is connected to input,

$$V_o = V_1 \quad -②$$

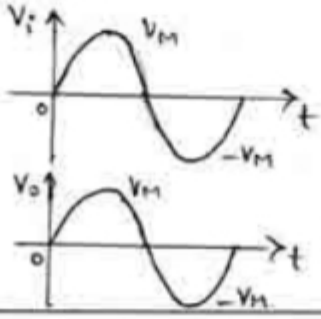
From ① & ②,

$$\boxed{V_o = V_i} \quad -③$$

Wave forms: DC



AC



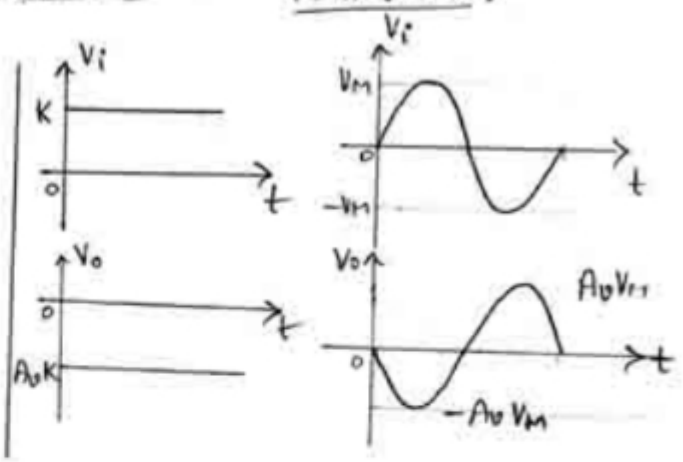
Conclusion:

- From eqn ③, the output voltage follows the input voltage

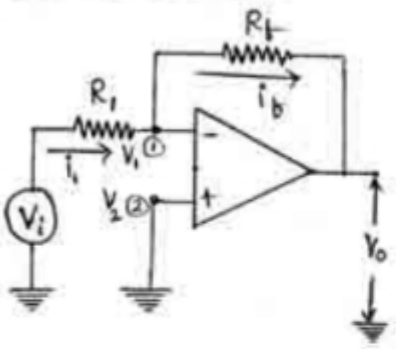
② Inverting amplifier:

Definition: An OP-amp circuit in which the output voltage is out of phase (180°) with respect to the input voltage is called inverting amplifier.

Waveforms:



Circuit diagram:



Analysis:

Applying KCL at node ①.

$$i_1 = i_f$$ (Since input impedance of OP-amp is very high, no current flows into OP-amp input terminals)

$$\Rightarrow \frac{V_i - V_1}{R_1} = \frac{V_1 - V_o}{R_f}$$

$$\Rightarrow \frac{V_i}{R_1} = \frac{-V_o}{R_f}$$ [From virtual ground concept, $V_1 = V_2 = 0$]

$$\Rightarrow \boxed{V_o = -\left(\frac{R_f}{R_1}\right) V_i} \quad -④ \quad \text{or} \quad \boxed{\frac{V_o}{V_i} = \frac{-R_f}{R_1} = A_v} \quad -⑤$$

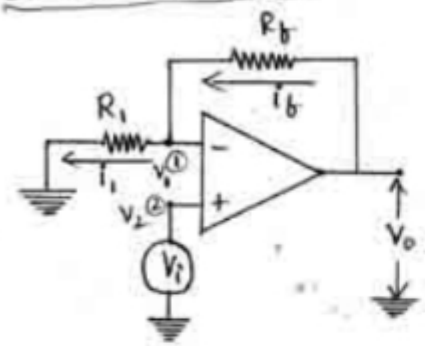
Where, $A_v \rightarrow$ Closed loop voltage gain

Conclusion: From eqn ⑤, negative sign indicates that the output is inverted w.r.t the input.

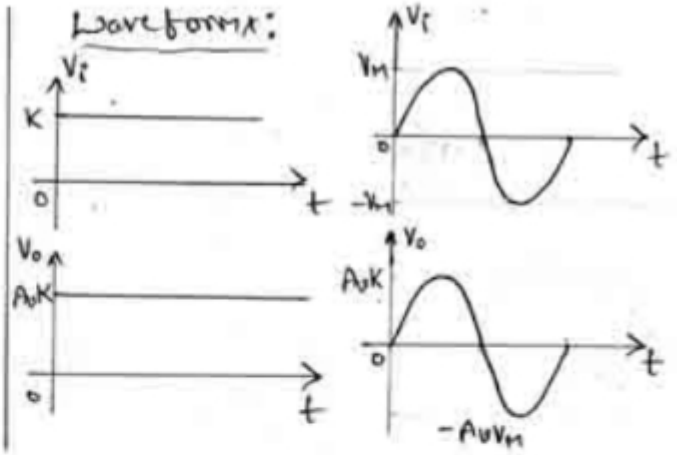
③ Non-inverting amplifier:

Definition: An OP-amp circuit in which the output voltage is in phase with the input voltage is called Non-inverting amplifier.

Circuit diagram:



Waveforms:



Analysis:

Applying KCL at node ①.

$$i_f = i_1 \quad (\because \text{No current flows into OP-amp input terminals})$$

$$\Rightarrow \frac{V_o - V_1}{R_f} = \frac{V_1 - 0}{R_1} \quad (\text{From virtual ground concept, } V_1 = V_2 = V_i)$$

$$\Rightarrow \frac{V_o - V_i}{R_f} = \frac{V_i}{R_1}$$

$$\Rightarrow \frac{V_o - V_i}{V_i} = \frac{R_f}{R_1}$$

$$\Rightarrow \frac{V_o}{V_i} - 1 = \frac{R_f}{R_1}$$

$$\Rightarrow \boxed{\frac{V_o}{V_i} = 1 + \frac{R_f}{R_1} = A_v} \quad -⑥ \qquad \boxed{V_o = \left(1 + \frac{R_f}{R_1}\right) V_i} \quad -⑦$$

Where, $A_v \rightarrow$ closed loop voltage gain.

Conclusion: From ⑥ ⑦ ⑧, • the output voltage is in-phase with the input voltage. • A_v depends on R_f & R_1

* (a) Summer (adder) (b) Summing amplifier:

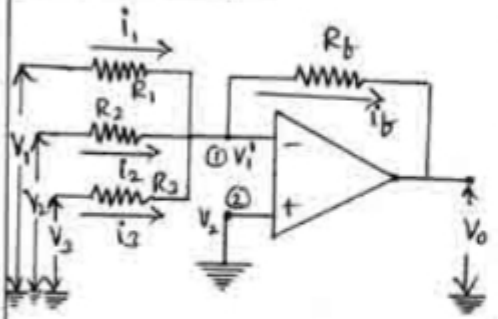
Definition: An op-amp circuit, in which the output voltage is the sum of the input signal voltages is called Summer.

There are two types:

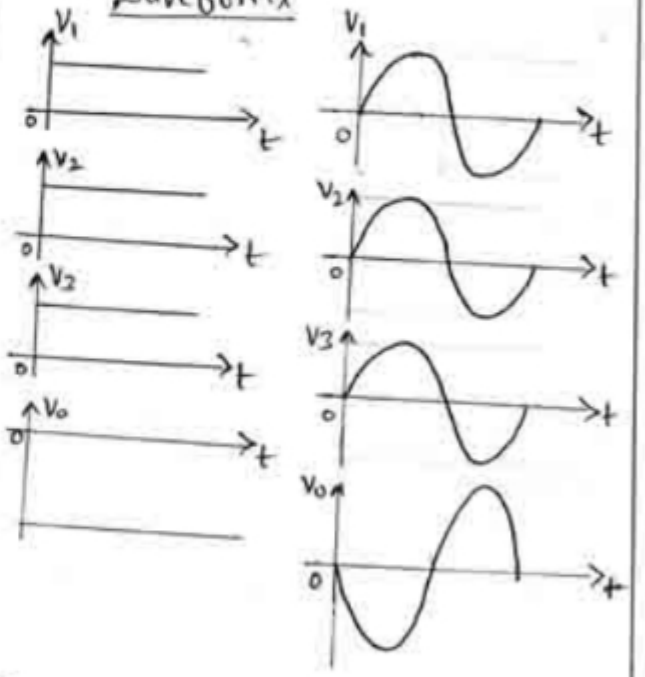
(a) Inverting summing amplifier:

Definition: An op-amp circuit, in which the output voltage is the inverted sum of the input voltages is called inverting summing amplifier.

Circuit diagram



Waveforms



Analysis:

Applying KCL at node ①.

$$i_1 + i_2 + i_3 = i_f \quad (\because \text{No current flows into op-amp input terminals})$$

$$\Rightarrow \frac{V_1 - V_1'}{R_1} + \frac{V_2 - V_1'}{R_2} + \frac{V_2 - V_1'}{R_3} = \frac{V_1' - V_o}{R_f}$$

$$\Rightarrow \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_2}{R_3} = -\frac{V_o}{R_f} \quad (\text{From virtual ground concept, } V_1' = V_2 = 0)$$

$$\Rightarrow \boxed{V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)} \quad -(8)$$

Conclusion:
From (8), the output voltage is proportional to the inverted sum of the input voltages.

Note:
(1) From (4), • If $R_f = R_1$, $V_o = -V_i$ (or) $\frac{V_o}{V_i} = -1 = A_v$ amplifier is unity gain inverting amplifier.

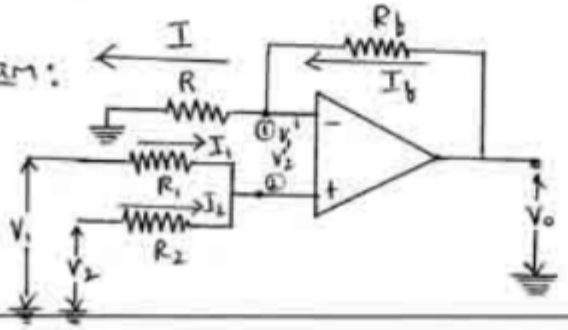
(2) From (7), • Irrespective of the value of R_1 & R_f, $V_o \geq V_i$
• If $R_f = 0$ (or) $R_1 = \infty$, then $V_o = V_i$, amplifier is unity gain non-inverting amplifier.

(3) From (8), • If $R_1 = R_2 = R_3 = R_f$, then, $V_o = -(V_1 + V_2 + V_3)$ output voltage is the negative of the sum of the input voltages [Gain of the Summer is unity (1)]
• If $R_1 = R_2 = R_3 = 3R_f$, then, $V_o = -\left(\frac{V_1 + V_2 + V_3}{3}\right)$
(or) $R_1 = R_2 = 2R_f$ & $V_3 = 0$, then $V_o = -\left(\frac{V_1 + V_2}{2}\right)$
then circuit is averager (or) averaging circuit

(5) Non-inverting Summer:

Definition: An OP-amp circuit, in which the output voltage is the sum of the input voltages is called Non-inverting Summer.

Circuit diagram:



Analysis:

Applying KCL at node ②

$$I_1 + I_2 = 0 \quad \text{(No current flows into input)}$$

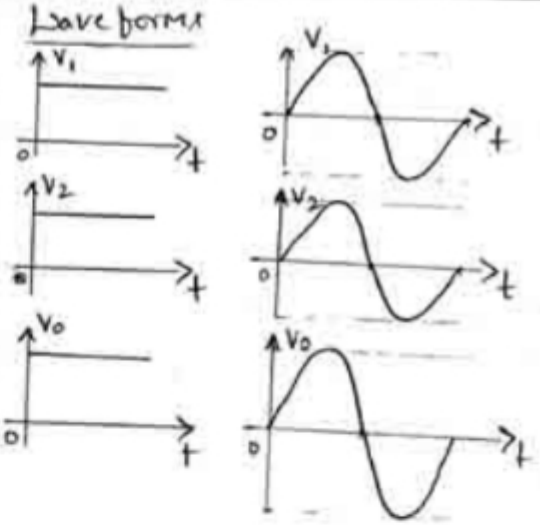
$$\Rightarrow \frac{V_1 - V_2'}{R_1} + \frac{V_2 - V_2'}{R_2} = 0$$

$$\Rightarrow \frac{V_1}{R_1} + \frac{V_2}{R_2} = V_2'\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$$

$$\Rightarrow \frac{R_2 V_1 + R_1 V_2}{R_1 R_2} = V_2'\left(\frac{R_2 + R_1}{R_1 R_2}\right)$$

$$\Rightarrow V_2' = \frac{R_2 V_1 + R_1 V_2}{R_1 + R_2} \quad -(9)$$

Waveforms



Applying KCL at node ①.

$$I_f = I$$

$$\Rightarrow \frac{V_o - V_1'}{R_f} = \frac{V_1' - 0}{R}$$

$$\Rightarrow \frac{V_o}{R_f} = V_1'\left(\frac{1}{R} + \frac{1}{R_f}\right)$$

$$\Rightarrow \frac{V_o}{R_f} = V_1'\left(\frac{R_f + R}{R R_f}\right)$$

$$V_o = V_1'\left(\frac{R + R_f}{R}\right) \quad -(10)$$

(From Virtual ground, $V_1' = V_2' = \frac{R_2 V_1 + R_1 V_2}{R_1 + R_2}$)

$$\Rightarrow V_o = \left(\frac{R_2 V_1 + R_1 V_2}{R_1 + R_2}\right)\left(\frac{R + R_f}{R}\right)$$

$$\Rightarrow V_o = \frac{R_2(R + R_f)}{R(R_1 + R_2)} V_1 + \frac{R_1(R + R_f)}{R(R_1 + R_2)} V_2$$

$$\Rightarrow \boxed{V_o = \frac{(1 + R_f/R)}{(1 + R_1/R_2)} V_1 + \frac{(1 + R_f/R)}{(1 + R_2/R_1)} V_2} \quad -(11)$$

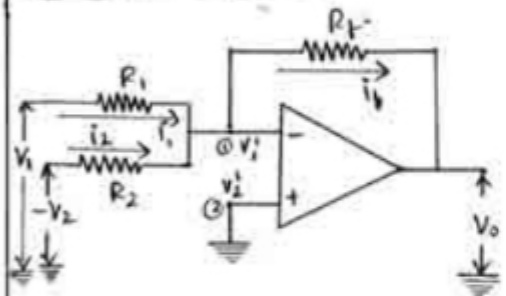
Conclusion:
From (11), the output voltage is proportional to the sum of the input voltages.

Note: ① From (11). If $R = R_f = R_1 = R_2$, $V_o = V_1 + V_2$ output voltage is equal to the non-inverted sum of the input voltages ② From (8), if $V_1, V_2 \& V_3$ are negative, $V_o = \frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3$

* (5) Subtractor (or) Difference amplifier

Definition: An op-amp circuit, in which the output voltage is the difference (subtraction) of two input voltages is called Subtractor.

Circuit diagram:



Applying KCL at node ①.

$$i_1 + i_2 = i_f$$

$$\Rightarrow \frac{V_1 - V_1'}{R_1} + \frac{-V_2 - V_1'}{R_2} = \frac{V_1' - V_o}{R_f}$$

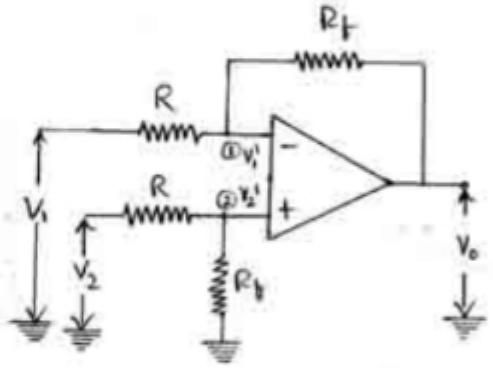
$$\Rightarrow \frac{V_1}{R_1} - \frac{V_2}{R_2} = -\frac{V_o}{R_f} \quad (\because V_1' = V_2' = 0)$$

$$\Rightarrow \boxed{V_o = \frac{R_f}{R_2}V_2 - \frac{R_f}{R_1}V_1} \quad -(12)$$

If $R_1 = R_2 = R_f$, then

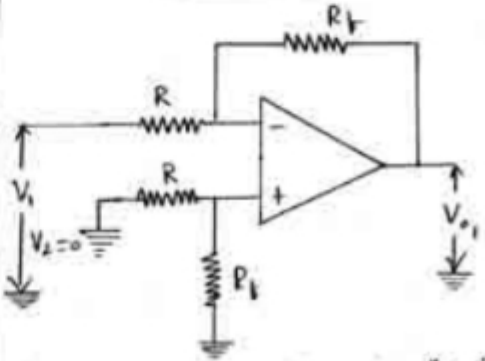
$$\boxed{V_o = V_2 - V_1} \quad -(13)$$

(or)



Let us use Superposition theorem.

Case (i): Let $V_2 = 0$



The resulting circuit is inverting amplifier

$$\therefore V_{o_1} = -\frac{R_f}{R}V_1 \quad -(14)$$

Case (ii): Let $V_1 = 0$

The resulting circuit is shown in fig (*)

The circuit is non-inverting amplifier.

$$\therefore V_{o_2} = \left(1 + \frac{R_f}{R}\right) V_2' \quad -(15)$$

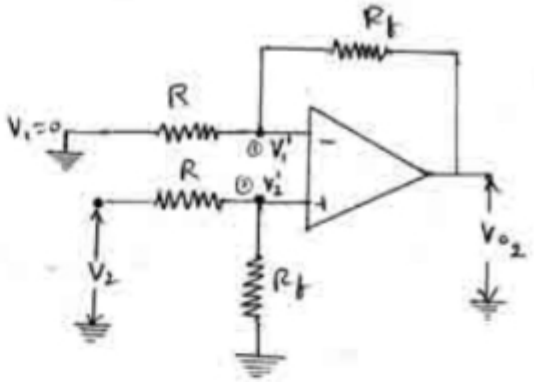


Fig (*):

From Potential divider rule

$$V_2' = \frac{V_2 R_f}{R + R_f} \quad -(16)$$

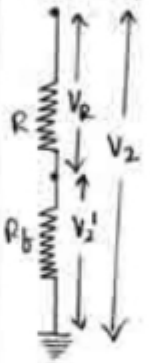
Using (16) in (15). We get

$$V_{o_2} = \left(1 + \frac{R_f}{R}\right) V_2 \left(\frac{R_f}{R + R_f}\right)$$

$$= \left(\frac{R + R_f}{R}\right) V_2 \left(\frac{R_f}{R + R_f}\right)$$

$$V_{o_2} = \frac{R_f}{R} V_2 \quad -(17)$$

Voltage @ Potential divider rule



Voltage across R_f.

$$V_2' = \frac{V_2 \times R_f}{R + R_f}$$

Voltage across R.

$$V_R = \frac{V_2 R}{R + R_f}$$

From Superposition theorem, the output voltage is

$$V_o = V_{o_1} + V_{o_2}$$

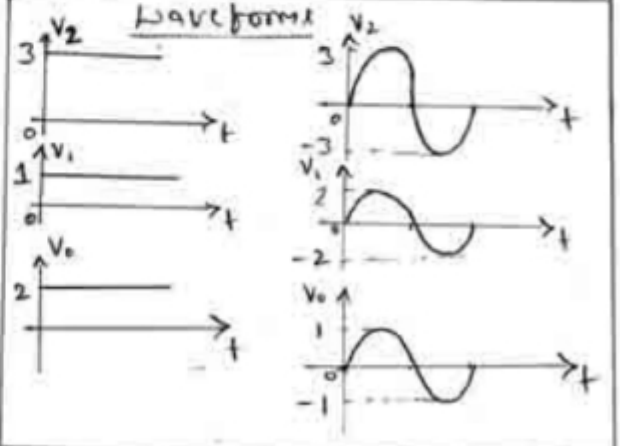
$$= -\frac{R_f}{R} V_1 + \frac{R_f}{R} V_2$$

$$\boxed{V_o = \frac{R_f}{R}(V_2 - V_1)} \quad -(18)$$

If $R = R_f$, then

$$\boxed{V_o = V_2 - V_1} \quad -(19)$$

Waveforms

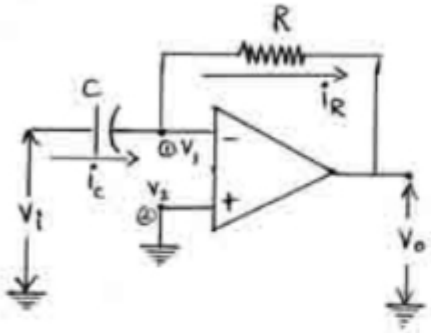


Conclusion: From (13) & (19), the output voltage is the difference of the two input voltages.

* ⑥ Differentiator:

Definition: An op-amp circuit, in which the output voltage is the differentiation (dairative) of the input voltage is called differentiator.

Circuit diagram



Analysis:

Applying KCL at node ①.

$$i_c = i_R$$

$$C\frac{d(V_i - V_1)}{dt} = \frac{V_1 - V_o}{R}$$

$$\Rightarrow C\frac{dV_i}{dt} = \frac{-V_o}{R} \quad (\because \text{From virtual ground concept, } V_1 = V_2 = 0)$$

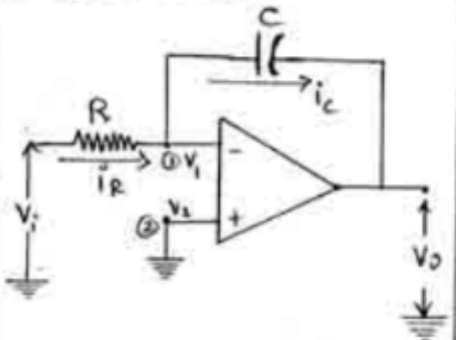
$$\Rightarrow \boxed{V_o = -RC\frac{dV_i}{dt}} \quad \text{—(20)}$$

Conclusion: From (20), the output voltage is proportional to the time dairative of the input voltage.

* ⑦ Integrator:

Definition: An op-amp circuit, in which the output voltage is the integration of the input voltage is called integrator

Circuit diagram:



Analysis:

Applying KCL at node ①.

$$i_R = i_c$$

$$\frac{V_i - V_1}{R} = C\frac{d(V_1 - V_o)}{dt}$$

$$\Rightarrow \frac{V_i}{R} = -C\frac{dV_o}{dt} \quad (\text{From virtual ground concept, } V_1 = V_2 = 0)$$

$$\Rightarrow dV_o = -\frac{1}{RC}V_i\,dt$$

Integrating on b.s.

$$V_o = -\frac{1}{RC}\int_0^t V_i\,dt + V_o(0) \quad -(21)$$

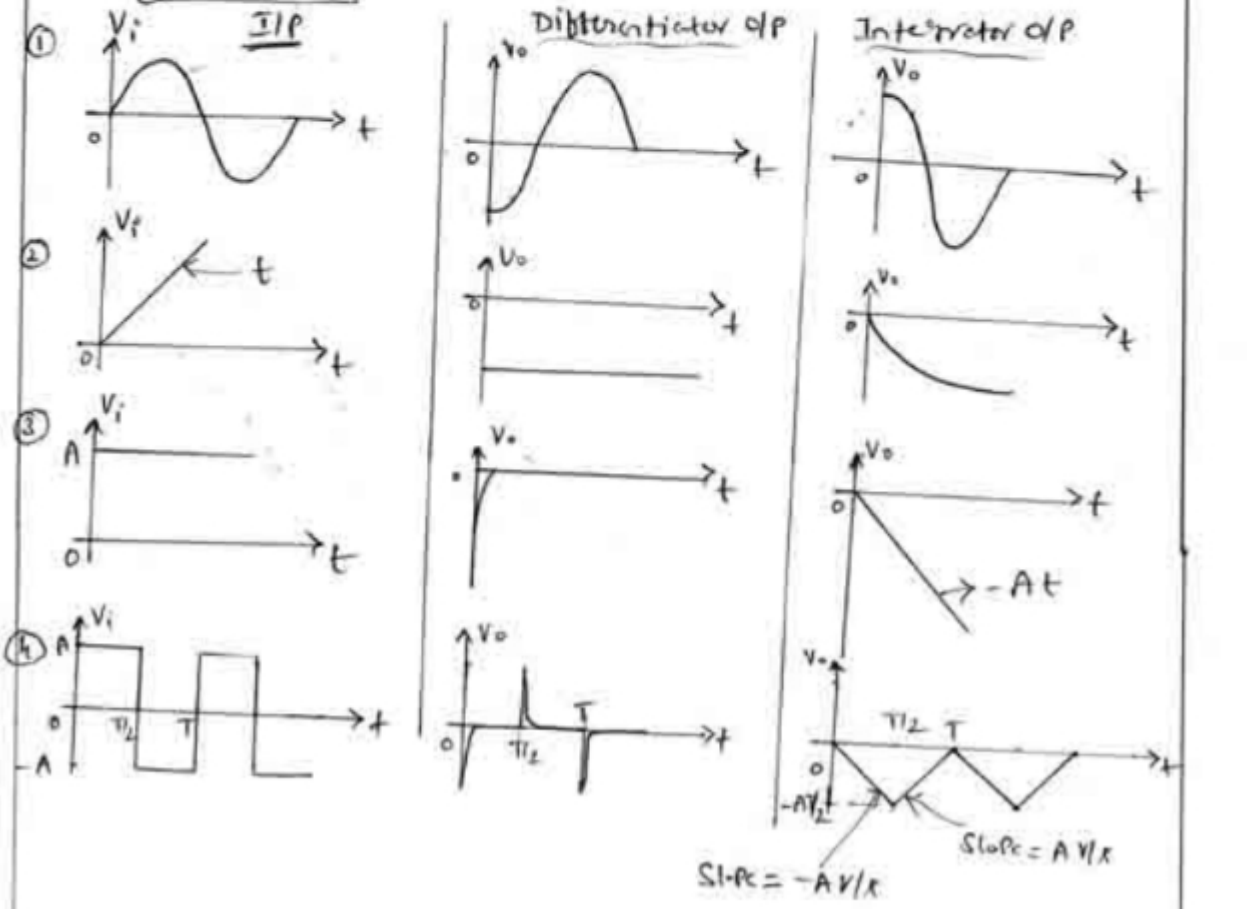
Where, $V_o(0)$ → Initial Voltage on capacitor at $t=0$
(Constant of integration)

If $V_o(0)=0$, then

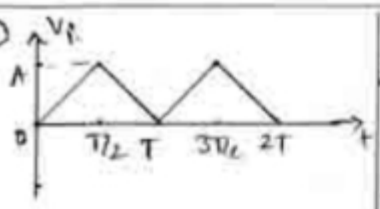
$$V_o = -\frac{1}{RC}\int_0^t V_i\,dt \quad -(22)$$

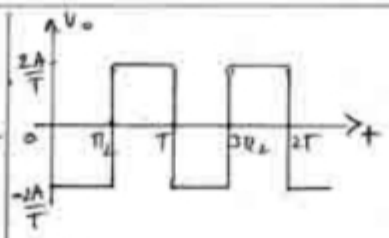
Conclusion: From (21) & (22), the output voltage is proportional to the integral of the input voltage.

Note: (1) Waveforms

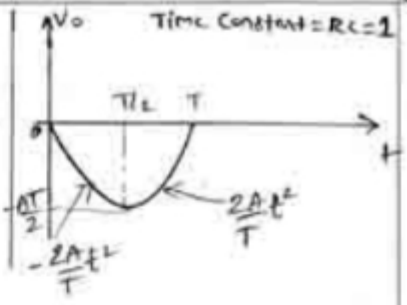


(5)





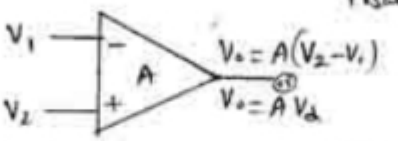
etc



(II) Ideal Voltage transfer characteristic of an OP-amp

The output voltage,

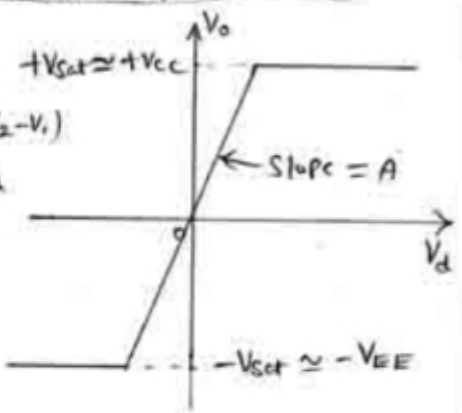
$V_o = A V_d$



Fig(*):

From characteristics

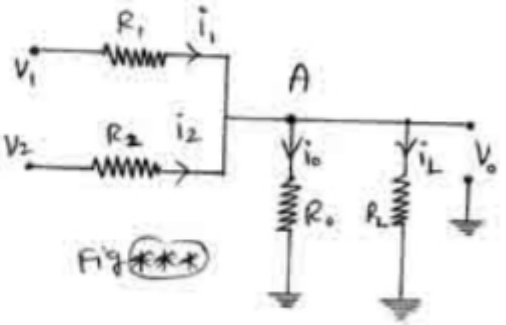
- As V_d increases, V_o increases linearly until it attains the saturation voltages & thereafter it remains constant.



Fig(**): Ideal voltage transfer characteristic of an OP-amp

(III) Need for an OP-amp

Let two signals V_1 & V_2 to be summed as shown in fig(***)



Fig(***)

Applying KCL at node A

$$i_1 + i_2 = i_o + i_L$$

$$\Rightarrow \frac{V_1 - V_o}{R_1} + \frac{V_2 - V_o}{R_2} = \frac{V_o}{R_o} + \frac{V_o}{R_L}$$

$$\Rightarrow \frac{V_1}{R_1} + \frac{V_2}{R_2} = V_o\left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_o} + \frac{1}{R_L}\right]$$

$$\Rightarrow V_o\left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_f}\right] = \frac{V_1}{R_1} + \frac{V_2}{R_2}$$

$$\Rightarrow V_o\left[1+\frac{R_p}{R_1}+\frac{R_p}{R_2}\right]=V_1\left(\frac{R_p}{R_1}\right)+V_2\left(\frac{R_p}{R_1}\right) \quad \boxed{\text{where } R_p=\frac{1}{R_o}+\frac{1}{R_L}}$$

$$\Rightarrow \boxed{V_o=\frac{V_1\left(\frac{R_p}{R_1}\right)+V_2\left(\frac{R_p}{R_1}\right)}{\left[1+\frac{R_p}{R_1}+\frac{R_p}{R_2}\right]}} \quad \text{—} (*)$$

From eqn (*), it is clear that V_o depends on R_p which inturn depends on R_L.

It is desirable to make V_o independent of R_L. This is possible if $R_o \ll R_L$ @ $\frac{1}{R_o} \gg \frac{1}{R_L}$ $\left(R_p \simeq \frac{1}{R_o}\right)$

But R_p will be small, results in small value of V_o which is undesirable. Therefore it is necessary to use amplifier whose gain (or output voltage) is independent of R_L.

Thus op-amp is preferred since closed loop voltage gain (@ output voltage) is independent of R_L (depends only on external resistors R_f & R_1).

① For an inverting amplifier $R = 10k\Omega$ & $R_f = 60k\Omega$. What is the output voltage for $V_i = 2V$?

Sol: Given $R = 10k\Omega$, $R_f = 60k\Omega$, $V_i = 2V$, $V_o = ?$

For an inverting amplifier,

$$V_o = -\frac{R_f}{R} V_i = -\frac{60\times10^3}{10\times10^3}(2) = -12V$$

② Design an inverting amplifier for output voltage of $-10V$ & an input voltage of $1V$.

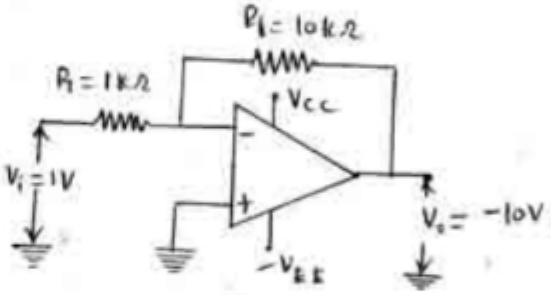
Sol: Given $V_o = -10V$, $V_i = 1V$, $R_1 = ?$ $R_f = ?$

For an inverting amplifier,

$$V_o = -\frac{R_f}{R_1} V_i$$

$$\Rightarrow -10 = -\frac{R_f}{R_1}(1)$$

$$\Rightarrow \frac{R_f}{R_1} = 10$$



Assume $R_1 = 1k\Omega$ //..

$\therefore R_f = 10k\Omega$ //..

③ The output signal of an OP-amp with a slew-rate of $5V/\mu s$ has a maximum value of $15V$. Find the max freq for undistorted output voltage

Sol: Given $SR = 5V/\mu s$ $V_m = 15V$, $f_{max}(\omega_{max}) = ?$

We have $f_{max} = \frac{SR}{2\pi V_m}$ $\omega_{max} = \frac{SR}{V_m}$

$= \frac{5/10^{-6}}{2\pi(15)}$ $\omega_{max} = \frac{5/10^{-6}}{15}$

$f_{max} = 53.05\ KHz$ @ $\omega_{max} = 333.33\ rad/s$

(4) Determine the output voltage of an OP-amp for the input voltages of 0.05mV & 0.04mV. The differential gain of the amplifier is 50000 & CMRR = 2×10^5.

Sol: Given $V_o = ?$, $V_1 = 0.05mV$, $V_2 = 0.04mV$, $A_d = 50000$, $CMRR = 2 \times 10^5$

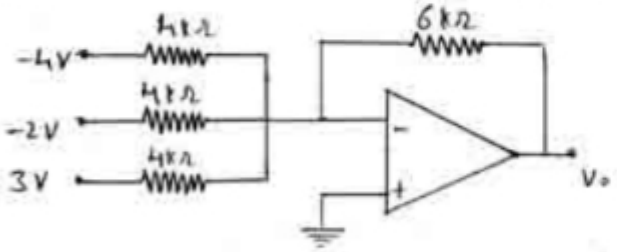
We have,

$$V_o = A_d V_d + A_c V_c$$
$$= 50000 \times 10 \times 10^{-6} + 0.25 \times 45 \times 10^{-6}$$
$$= 0.5 + 11.25 \times 10^{-6}$$
$$= 500.011\ mV$$

$\because V_d = V_1 - V_2$
$= 0.05 \times 10^{-3} - 0.04 \times 10^{-3}$
$= 0.01 \times 10^{-3} = 10 \times 10^{-6}$

$A_c = \frac{A_d}{CMRR} = \frac{50000}{2 \times 10^5} = 0.25$

(5) Find the output voltage for the circuit shown in fig (5)



Sol: We have, $V_o = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right)$

$= -\frac{R_f}{R_1}(V_1 + V_2 + V_3)$ $\left(\because R_1 = R_2 = R_3 = 4k\Omega\right)$

$= -\frac{6k\Omega}{4k\Omega}(-4 - 2 + 3)$

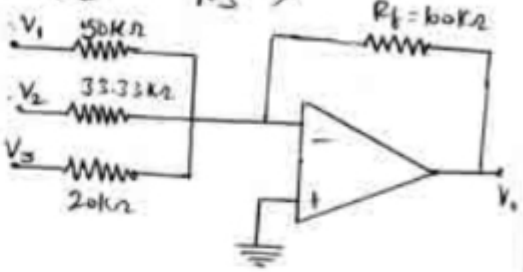
$= 4.5V$

(6) Design an adder circuit for $V_o = -[2V_1 + 3V_2 + 5V_3]$

Sol: Given $V_o = -(2V_1 + 3V_2 + 5V_3)$

Comparing with $V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$

$\frac{R_f}{R_1} = 2$, $\frac{R_f}{R_2} = 3$, $\frac{R_f}{R_3} = 5$



Let $R_f = 100\,k\Omega$

$\therefore R_1 = \frac{R_f}{2}$ $R_2 = \frac{R_f}{3}$ $R_3 = \frac{R_f}{5}$

$\Rightarrow R_1 = 50k\Omega$ $R_2 = 33.33k\Omega$ $R_3 = 20k\Omega$

(7) Design an adder circuit for $V_o = 3V_1 + 2V_2 - 4V_3$

Sol: Given $V_o = 3V_1 + 2V_2 - 4V_3$

$\Rightarrow V_o = -[3(-V_1) + 2(-V_2) + 4V_3]$

Comparing with

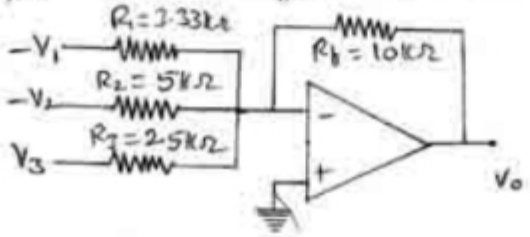
$$V_o = -\left[\frac{R_f}{R_1}(-V_1) + \frac{R_f}{R_2}(-V_2) + \frac{R_f}{R_3}V_3\right]$$

$\frac{R_f}{R_1} = 3$, $\frac{R_f}{R_2} = 2$, $\frac{R_f}{R_3} = 4$

Let $\boxed{R_f = 10\,k\Omega}$

$\therefore R_1 = \frac{10k}{3}$, $R_2 = \frac{10k}{2}$, $R_3 = \frac{10k}{4}$

$\boxed{R_1 = 3.33k\Omega}$ $\boxed{R_2 = 5k\Omega}$ $\boxed{R_3 = 2.5k\Omega}$



(8) A differential amplifier has open circuit gain of 10^4, the input signals are 1.2MV & 2.4MV. Determine the output voltage.

Sol: Given $A_d = 10^4$, $V_2 = 2.4 \times 10^{-6}V$, $V_1 = 1.2 \times 10^{-6}V$, $V_o = ?$

output voltage, $V_o = A_d V_d$

$= A_d(V_2 - V_1)$ (∵ since Ac is not given)

$= 10^4(2.4 - 1.2) \times 10^{-6}$

$= 0.012V$

(9) For the circuit shown in fig (a). draw the output voltage for the input voltage shown in fig (b)

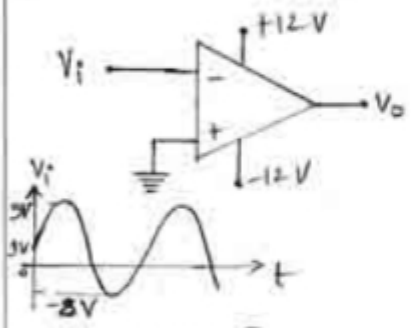


Fig 19(a)

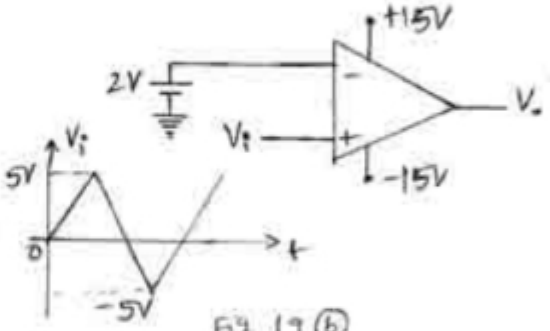
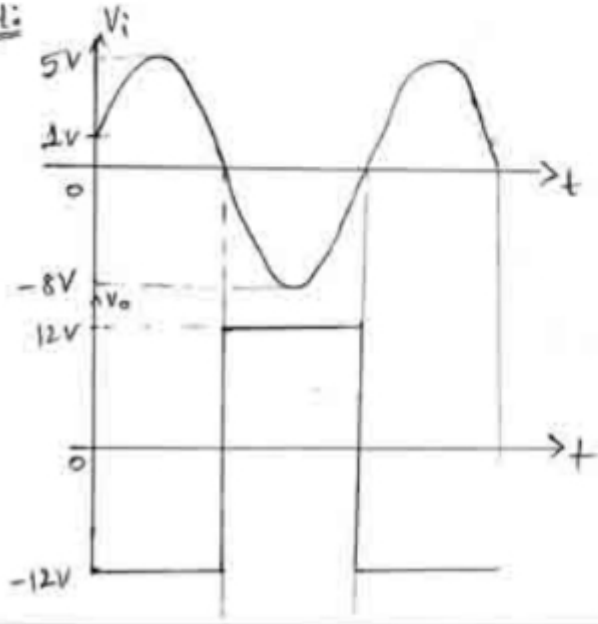
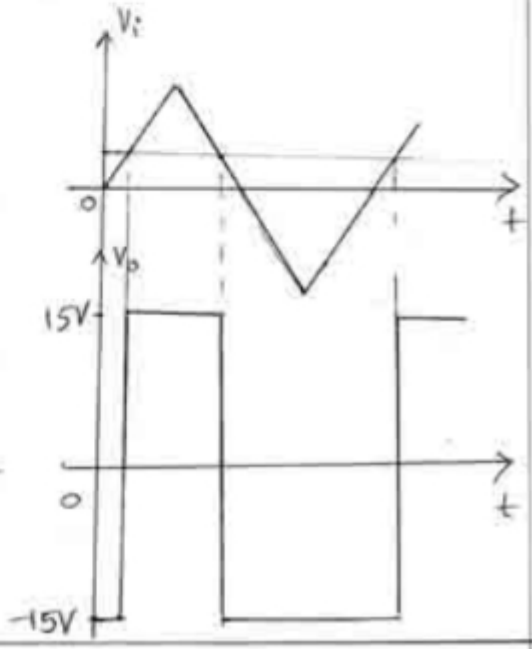


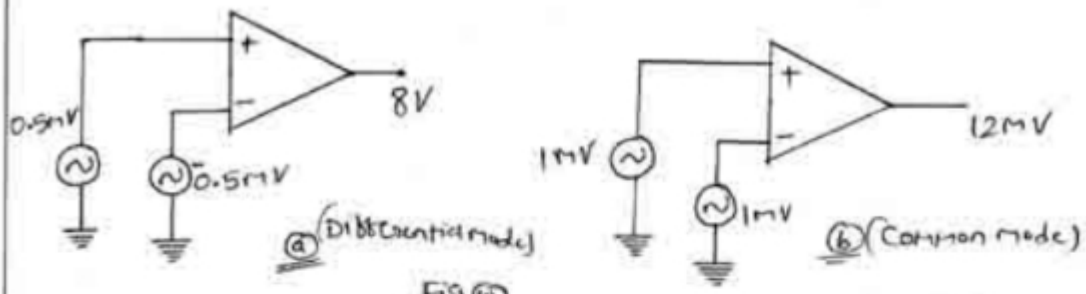
Fig 19 (b)

Sol:





(10) Calculate the CMRR for the circuit measurements shown in fig(10).

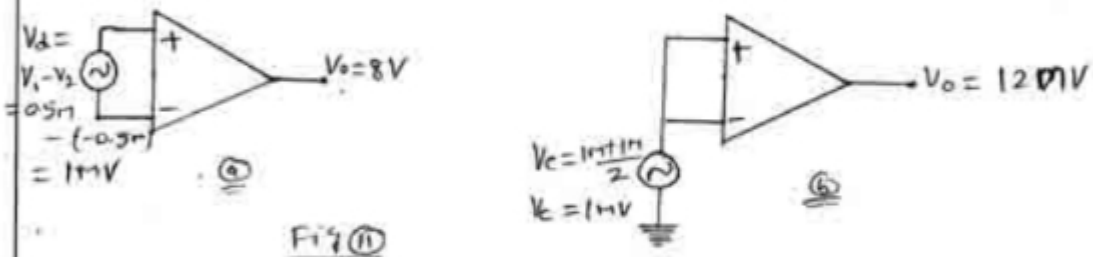


(a) (Differential mode) (b) (Common mode)

Fig(10)

Sol:

Fig 10(a) can be redrawn as shown in fig 11(a) & fig 10(b) can be redrawn as shown in fig 11(b).



(a) (b)

Fig(11)

From fig(10)(a),

$$A_d = \frac{V_o}{V_d} = \frac{8}{1\times10^{-3}} = 8000$$

From fig(10)(b),

$$A_c = \frac{V_o}{V_c} = \frac{12\times10^{-3}}{1\times10^{-3}} = 12$$

∴ CMRR is,

$$CMRR = \frac{A_d}{A_c} = \frac{8000}{12} = 666.66$$

(or)

$$CMRR\,(dB) = 20\log_{10}\frac{A_d}{A_c} = 20\log_{10}(666.66) = 56.47dB$$

(11) Determine the output voltage of an OP-amp for input voltages of $V_{i1} = 150\mu V$, $V_{i2} = 140\mu V$. The amplifier has a differential gain of $A_d = 4000$ & the value of CMRR is:

(a) 100 (b) 10^5.

Sol: Difference voltage, $V_d = V_{i1} - V_{i2} = 150\times10^{-6} - 140\times10^{-6} = 10\mu V$

Common mode voltage, $V_c = \frac{V_{i1}+V_{i2}}{2} = \frac{150\times10^{-6} + 140\times10^{-6}}{2} = 145\mu V$

(a) We have, $V_o = A_d V_d \left(1 + \frac{1}{CMRR}\frac{V_c}{V_d}\right)$

$= (4000)(10\times10^{-6})\left(1 + \frac{1}{100}\frac{14.5\times10^{-6}}{10\times10^{-6}}\right)$

$= 40\times10^{-3}(1 + 0.145)$

$= 45.8\,mV$

(b) $V_o = (4000)(10\times10^{-6})\left(1 + \frac{1}{10^5}\frac{145\times10^{-6}}{10\times10^{-6}}\right)$

$= 40\times10^{-3}(1.000145)$

$= 40.0058\,mV$

(12) Calculate the output voltage of a non-inverting amplifier for $V_i = 2V$, $R_f = 500\,k\Omega$ & $R_i = 100\,k\Omega$

Sol: Given $V_i = 2V$, $R_f = 500\,K\Omega$, $R_i = 100\,K\Omega$, $V_o = ?$

For non-inverting amplifier,

$$V_o = \left(1 + \frac{R_f}{R_i}\right)V_i = \left(1 + \frac{500\times10^3}{100\times10^3}\right)2 = 6(2) = 12V$$

(13) A 741C is an OP-AMP with $A = 100,000$ & a minimum $CMRR_{dB} = 70dB$. What is the common-mode voltage gain? If a desired common-mode signal each has a value of 5MV, what is the output voltage?

Sol: Given $A = A_d = 100.000$, $CMRR(dB) = 70dB$, $A_c = ?$

$V_c = 5\times10^{-6}V$, $V_o = ?$

We have $CMRR(dB) = 20\log_{10}\frac{A}{A_c}$

$\Rightarrow \quad 70 = 20\log_{10}\frac{A}{A_c}$

$\Rightarrow \quad \frac{A}{A_c} = 10^{70/20}$

$\Rightarrow \quad A_c = \frac{A}{10^{7/2}} = \frac{100.000}{10^{7/2}} = 31.622$

We have $V_o(CM) = A_c V_c$

$= 31.622 \times 5 \times 10^{-6}$

$V_o(CM) = 158.11 \mu V$

(14) Assume that negative saturation occurs at 1V less than the supply voltage with an op-amp. How much inverting input voltage does it take to drive the op-amp of fig (14) into negative saturation?

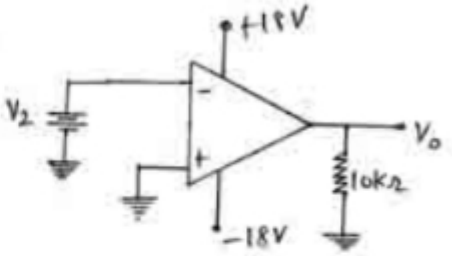


Fig (14)

Sol: Given $V_{cc} = \pm 18V$, Negative Saturation Voltage $= -17V$

$V_2 = ?$ $A = 2 \times 10^5$ (Assume)

Given negative saturation voltage $= -17V$, output saturates negatively at $-17V$.

$\therefore V_2 = \frac{17}{200,000} = 85 \mu V$ $\quad [\because V_o = A V_2]$

(15) The input voltage to an op-amp is a large voltage step. The output is an exponential waveform that changes 0.75V in 50ns. What is the slew rate of the op amp?

Sol: Given $dV = 0.75V$, $dt = 50ns$

We have, $SR = \frac{dV}{dt} = \frac{0.75}{50 \times 10^{-9}} = 15V/\mu s$

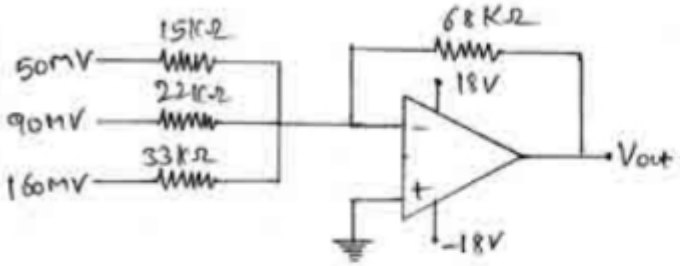
(16) An op-amp has slew rate of $8V/\mu s$. What is the power bandwidth for a peak output voltage of 5V?

Sol: Given $SR = 8V/\mu s$, $V_m = 5V$, $f_{max} = ?$

Highest freq @ power bandwidth,

$$f_{max} = \frac{SR}{2\pi V_m} = \frac{\cdot 8/10^{-6}}{2\pi \times 5} = 254.64\,KHz$$

(17) In fig (16). What is the ac output voltage? If a compensating resistor needs to be added to non-inverting input, what size should it be?



Sol:

AC output voltage,

$$V_o = \left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

$$= \left[\frac{68K}{15K}(50\times10^{-3}) + \frac{68K}{22K}(90\times10^{-3}) + \frac{68K}{33K}(160\times10^{-3})\right]$$

$$= 834.53\,mV$$

Compensating resistor,

$$R_c = R_1 \| R_2 \| R_3$$

$$= \frac{1}{\frac{1}{15K} + \frac{1}{22K} + \frac{1}{33K}}$$

$$= 7.02\,K\Omega$$

[If a summing circuit needs to be compensated by adding an equal resistance to the non-inverting input, the resistance is the Thevenin resistance looking from the inverting input back to the sources]

(18) What is the initial slope of a sine wave with a frequency of 15KHz & a peak value of 2V? What happens to the initial slope if the frequency increases to 30KHz?

Sol: Given (a) $f = 15KHz$, $V_m = 2V$, $S_s(SR) = ?$

Initial slope of a sine wave.

$$S_s = 2\pi f V_m \qquad (\because SR = S_s = 2\pi f V_m)$$
$$= 2\pi \times 15 \times 10^3 \times 2$$
$$= 188.49 mV/\mu s$$

(b) $f = 30KHz$, $V_m = 2V$, $S_s = ?$

$$S_s = 2\pi f V_m = 2\pi \times 30 \times 10^3 \times 2 = 376.99 mV/\mu s$$

19) Find V_{out} in fig (19), if $R = 10k\Omega$, $V_1 = -20mV$, $V_2 = -30mV$

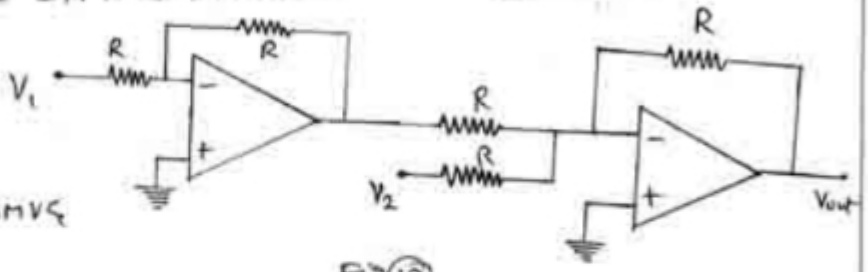
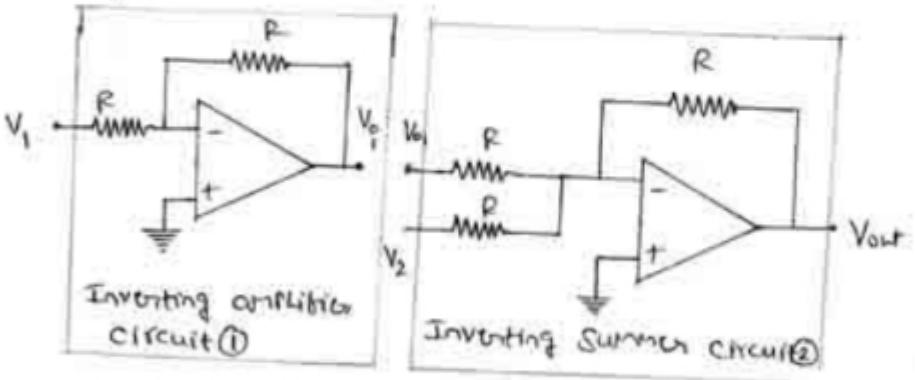


Fig (19)

Sol:

The given circuit is redrawn



From circuit (1),

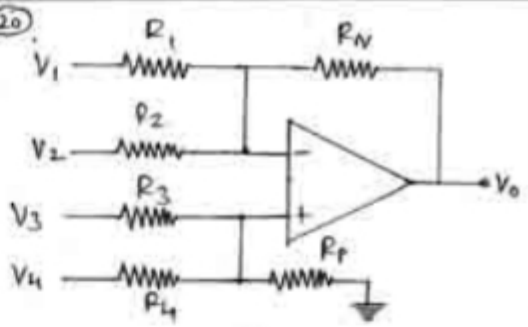
$$V_{o_1} = -\frac{R}{R} V_1$$
$$= -(-20mV)$$
$$= 20mV$$

From circuit (2)

$$V_{out} = -\left(\frac{R}{R} V_{o_1} + \frac{R}{R} V_2\right) \quad \text{or} \quad V_{out} = V_2 - V_{o_1}$$
$$= -(20mV - 30mV)$$
$$= -20mV + 30mV$$
$$V_{out} = 10mV$$

The given circuit is a subtractor

5) In the op-amp circuit of fig(20). Show that $V_o = (V_3 + V_4) - (V_1 + V_2)$ if all resistances are equal.

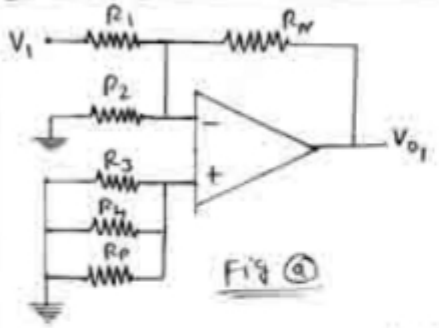


Fig(20)

Sol:

Let us use Superposition theorem.

Case(i): Let $V_2 = V_3 = V_4 = 0$



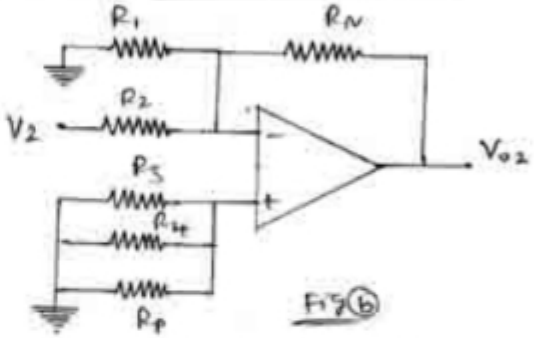
Fig(a)

The resulting circuit is shown in fig(a). The circuit is inverting amplifier. o/p V_{o1} is,

$$\therefore V_{o_1} = -\frac{R_N}{R_1} V_1$$

$$\boxed{V_{o_1} = -V_1} \quad (\text{Let } R_1 = R_N) \quad -(1)$$

Case(ii): Let $V_1 = V_3 = V_4 = 0$



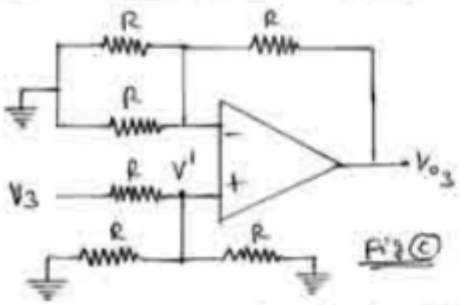
Fig(b)

The output voltage V_{o2} is,

$$V_{o_2} = -\frac{R_N}{R_2} V_2$$

$$\boxed{V_{o_2} = -V_2} \quad -(2) \quad (\text{Let } R_2 = R_N)$$

Case(iii): Let $V_1 = V_2 = V_4 = 0$

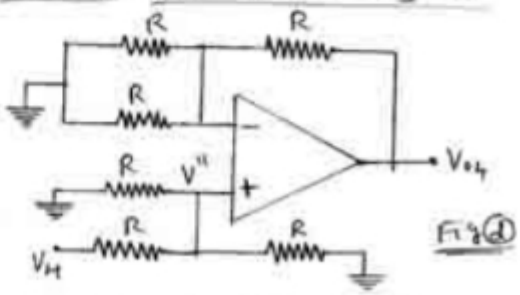


Fig(c)

From potential divider rule,

$$V' = \frac{V_3 (R \| R)}{R + (R \| R)}$$

Case(iv): Let $V_1 = V_2 = V_3 = 0$



Fig(d)

From potential divider rule,

$$V'' = \frac{V_4 (R \| R)}{R + (R \| R)}$$

$$V' = V_3 \frac{\frac{RR}{R+R}}{R + \frac{RR}{R+R}}$$

$$= V_3 \frac{\frac{R^2}{2R}}{R + \frac{R^2}{2R}}$$

$$= V_3 \frac{R/2}{3R/2}$$

$$= \frac{V_3}{3} \quad -(*)$$

Now Fig (c) can be redrawn as

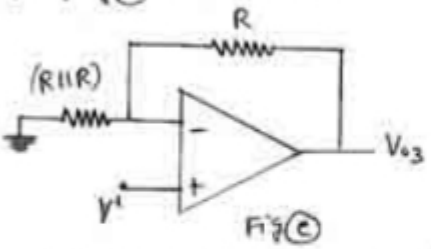


Fig (c)

The resulting circuit shown in fig (c) is non-inverting amplifier

∴ The output voltage V_{o3} is

$$V_{o3} = \left[1 + \frac{R}{(R||R)}\right] V' \quad -(***)$$

using (*) in (***)

$$V_{o3} = \left[1 + \frac{R}{(RR/R+R)}\right] \frac{V_3}{3}$$

$$= \left(1 + \frac{R}{R^2/2R}\right)\left(\frac{V_3}{3}\right)$$

$$= (1+2)\frac{V_3}{3}$$

$$\boxed{V_{o3} = V_3} \quad -(3)$$

$$\Rightarrow V'' = \frac{V_4 \; (RR/R+R)}{R + (RR/R+R)}$$

$$\Rightarrow V'' = \frac{V_4}{3} \quad -(**)$$

Similarly

$$V_{o4} = \left[1 + \frac{R}{(R||R)}\right] V''$$

$$\boxed{V_{o4} = V_4} \quad -(4)$$

From Superposition theorem, the output voltage is

$$V_o = V_{o1} + V_{o2} + V_{o3} + V_{o4} = (V_3 + V_4) - (V_1 + V_2)$$

(1) For the fig (21), determine V_o

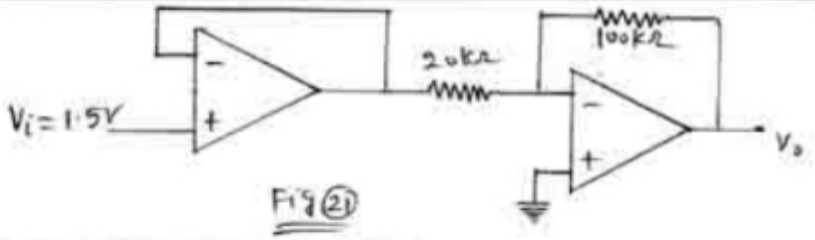
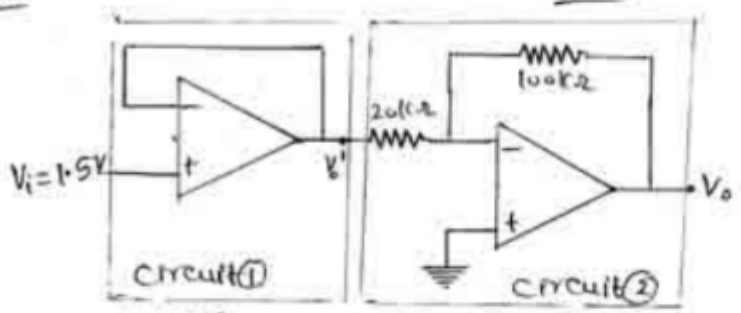


Fig (21)

Sol:



From circuit ①, o/p of voltage follower is,

$$V_o' = V_i = 1.5V$$

From circuit ②, output V_o is,

$$V_o = -\left(\frac{100K}{20K}\right)V_o' = -5(1.5) = -7.5V$$

(2) Determine the input bias current and input Offset current to an op-amp if the current into non-inverting and inverting terminals are 8.3 MA and 7.9 MA respectively.

Sol: Given $I_1 = 8.3MA$, $I_2 = 7.9MA$, $I_{ib} = ?$, $I_{io} = ?$

Input bias current, $I_{ib} = \frac{I_1 + I_2}{2} = \frac{8.3 + 7.7}{2} = 8.1MA$

Input offset current, $I_{io} = |I_1 - I_2| = |8.3 - 7.9| = 0.4MA$

(3) How long does it take the output voltage of an op-amp to go from $-8V$ to $7V$, if the slew rate is $0.5V/\mu s$?

Sol: Given $dV_o = 7 - (-8) = 15V$, $SR = \frac{0.5}{10^{-6}}$ V/s, $dt = ?$

We have $SR = \frac{dV_o}{dt} \Rightarrow dt = \frac{dV_o}{SR} = \frac{15}{0.5/10^{-6}} = 30\mu s$

4) For the inverting amplifier, $R_1 = 20k\Omega$, $R_f = 100k\Omega$, $V_{in} = 1mV$, Calculate
ⓐ Closed-loop gain ⓑ Input resistance seen by source ⓒ output voltage ⓓ Input current ⓔ current entering the op-amp input terminals ⓕ current through feedback.

Sol: Given, $R_1 = 20k\Omega$, $R_f = 100k\Omega$, $V_{in} = 1mV$, A (or A_f) = ?,
R_{in} = ?, I_{in} = ?, V_o = ?, $I_{op\text{-}amp}$ = ?, I_f = ?

ⓐ We have, $A = -\frac{R_f}{R_1} = -\frac{100 \times 10^3}{20 \times 10^3} = -5$ //.

ⓑ $R_{in} = R_1 = 20k\Omega$

ⓒ output voltage, $V_o = +AV_{in} = -5 \times 1 \times 10^{-3} = -5mV$

ⓓ $I_{in} = \frac{V_{in} - V_1}{R_1} = \frac{1 \times 10^{-3} - 0}{20 \times 10^3} = 50nA$ // [∵ From virtual ground, $V_1 = V_2 = 0$]

ⓔ $I_{op\text{-}amp} = 0$ (∵ No current flows into op-amp input terminals)

ⓕ $I_f = I_{in} = 50nA$

5) A sinusoidal signal with peak value 6mV & of 20KHz is applied to the input of an ideal op-amp integrator with $R = 100k\Omega$ & $C = 1MF$. Find the output voltage.

Sol: Given $R = 100K\Omega$, $C = 1MF$, $V_M = 6mV$, $f = 20KH?$, V_o = ?

$V_{in} = V_M \sin \omega t = 6 \times 10^{-3} \sin(2\pi f t) = 6 \times 10^{-3} \sin(40000\pi t)$

output voltage, $V_o = -\frac{1}{RC} \int_0^t V_{in} dt + V_o(0)$

$= -\frac{1}{100 \times 10^3 \times 1 \times 10^{-6}} \int_0^t 6 \times 10^{-3} \sin(40000\pi t)$

Assume $V_o(0) = 0$
Initial V/g across capacitor = 0

$$= -10\left[(6\times10^{-3})\left(\frac{-\cos 40000\pi t}{40000\pi}\right)_0^t\right]$$

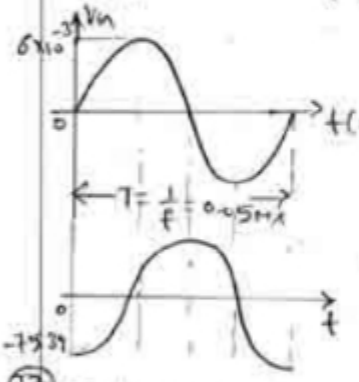
$$V_o = 477.46\,[\cos(40000\pi t) - 1]\ mV$$

(26) The input to a ideal differentiator is a sinusoidal voltage of peak voltage 6mV & frequency 20KHz. Find the output voltage, Given $R = 100K\Omega$ & $C = 1MF$.

Sol: Given $R = 100K\Omega$, $C = 1MF$, $V_M = 6mV$, $f = 20KHz$.

$$V_{in} = V_M \sin(\omega t) = 6\times10^{-3}\sin(40000\pi t)$$

output voltage, $V_o = -RC\frac{dV_{in}}{dt}$



$$= -100\times10^3\times1\times10^{-6}\frac{d}{dt}[6\times10^{-3}\sin(40000\pi t)]$$

$$= -0.1\times6\times10^{-3}\cos(40000\pi t).40000\pi$$

$$V_o = -75.39\cos(40000\pi t)\ V$$

(27) Determine the output voltage of a ideal differentiator for the input shown in fig (27). Given $RC = 1\mu s$.

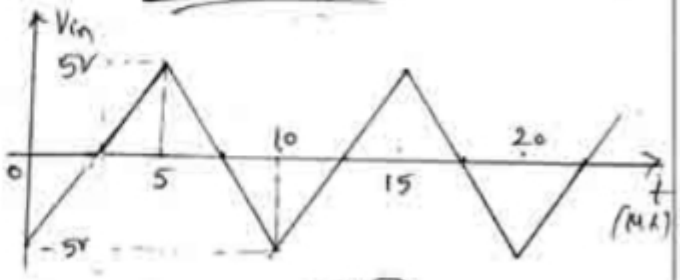
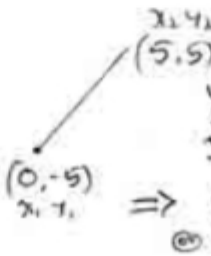


Fig (27)

Sol: Given $RC = 1\mu s$

case (i): For $0 < t < 5\mu s$

$$\frac{dV_{in}}{dt} = \frac{5-(-5)}{(5-0)} = 2V/\mu s$$



$$\frac{y_2-y_1}{x_2-x_1} = \frac{y-y_1}{x-x_1}$$

$$\Rightarrow y = 2x - 5$$

@ $V_{in} = 2t - 5$

Diff w.r.t t

$$\frac{dV_{in}}{dt} = 2\ V/\mu s$$

$$\therefore V_o = -RC\frac{dV_{in}}{dt} = -1\times10^{-6}\frac{2}{10^{-6}} = -2V$$

Case (ii): For $5\mu s < t < 10\mu s$

$$\frac{dV_{in}}{dt} = \frac{-5-5}{(10-5)} = \frac{-10}{5} = -2V/\mu s$$

(5,5) (x_1, y_1) and (10,-5) (x_2, y_2)

$$\frac{-5-5}{10-5} = \frac{y-5}{x-5}$$

$$\frac{-10}{5} = \frac{y-5}{x-5}$$

$$y-5 = -2x+10$$

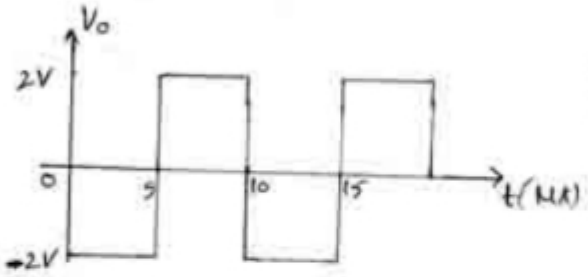
$$y = -2x+15$$

$$\frac{dy}{dx} = -2\ V/\mu s$$

$$\therefore V_o = -RC\frac{dV_{in}}{dt}$$

$$= -1\times10^{-6}\left(\frac{-2}{10^{-6}}\right)$$

$$= 2V$$



28) Calculate

(a) The output offset voltage due to input offset voltage = 1.2mV

(b) The output offset voltage due to input offset current = 100nA.

(c) The output offset voltage due to input offset voltage = 4mV & input offset current = 150nA.

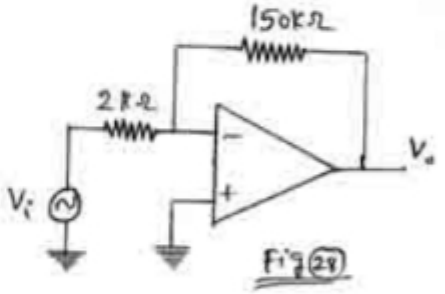


Fig 28

Sol:

(a) Given $V_{io} = 1.2mV$

output offset voltage.

$$V_{oo}(\text{due to } V_{io}) = V_{io}\left(\frac{R_1+R_f}{R_1}\right) = 1.2\times10^{-3}\left(\frac{2K+150K}{2K}\right)$$

$$V_{oo}(\text{due to } V_{io}) = 91.2mV$$

(b) V_{oo} (due to I_{io}) $= I_{io} R_f = 100\times10^{-9} \times 150\times10^{3} = 15\,mV$

(c) $V_{oo} = V_{oo}$(due to V_{io}) + V_{oo}(due to I_{io})

$= V_{io}\left(1 + \frac{R_f}{R_1}\right) + I_{io} R_f$

$= 4\times10^{-3}\left(1 + \frac{150K}{2K}\right) + 150\times10^{-9}(150K)$

$= 304\times10^{-3} + 22.5\times10^{-3}$

$= 326.5\,mV$

29) Calculate the input bias currents at each input of an op-amp having input bias current = 30nA & Input offset current = 5nA

Sol:

We have: $I_1 = I_{ib} + \frac{I_{io}}{2}$ & $I_2 = I_{ib} - \frac{I_{io}}{2}$

$= 30\times10^{-9} + \frac{5\times10^{-9}}{2}$ $= 30\times10^{-9} - \frac{5\times10^{-9}}{2}$

$= 32.5nA$ $= 27.5nA$

30) For an op-amp having a slew rate of 2V/μs, what is the maximum closed-loop voltage gain that can be used when the input signal varies by 0.5V in 10μs?

Sol: We have $V_o = A\,V_{in}$

$\Rightarrow dV_o = A\,dV_{in}$

$\Rightarrow \frac{dV_o}{dt} = A\frac{dV_{in}}{dt}$

$\Rightarrow A = \frac{dV_o/dt}{dV_{in}/dt} = \frac{SR}{dV_{in}/dt} = \frac{2/10^{-6}}{0.5/10\times10^{-6}} = 40$

Maximum closed-loop voltage gain = 40//.

31) For the signal & circuit of fig 31, determine the max frequency that may be used. Op-amp slew rate = 0.5 V/μs.

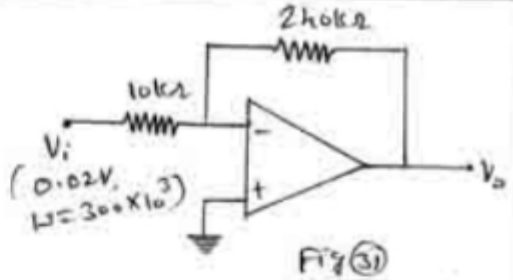


Fig 31

Sol:

Gain $A = \left|\frac{R_f}{R_1}\right| = \frac{240 \times 10^3}{10 \times 10^3} = 24$

Output Voltage (maximum)

$$V_M = A V_i = 24 \times 0.02 = 0.48\ V$$

We have $\omega_M \le \frac{SR}{V_M}$ @ $f_M \le \frac{SR}{2\pi V_M}$

$\le \frac{0.5/10^{-6}}{0.48}$ $\le \frac{0.5/10^{-6}}{2\pi \times 0.48}$

$\omega_M \le 1.041 \times 10^6$ rad/s @ $f_M \le 165.78$ KHz

Since the signal's frequency ($\omega = 300 \times 10^3$ rad/s) is less than the maximum freq ω_M, no output distortion will result.

32) For the circuit shown in fig 32.

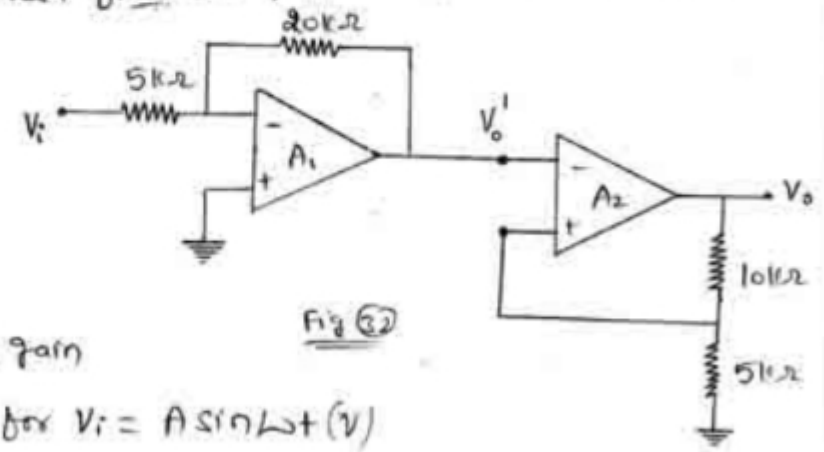


Fig 32

ⓐ Calculate A_1

ⓑ Calculate A_2

ⓒ Find the total gain

ⓓ Find V_o' & V_o for $V_i = A \sin \omega t$ (V)

Sol:

ⓐ $A_1 = -\frac{20k\Omega}{5k} = -4$ ⓑ $A_2 = 1 + \frac{10k\Omega}{5k} = 3$

ⓒ $A = A_1 A_2 = -12$

(d) $V_o' = (-2)\, A \sin \omega t = -2A \sin \omega t$ (V)

$V_o = A_2 V_o' = 3(-2A \sin \omega t) = -6A \sin \omega t$ (V)

33) Design an op-amp circuit for $V_o = 2V_1 - 3V_2 + 4V_3 - 5V_4$

Sol: $V_o = 2V_1 - 3V_2 + 4V_3 - 5V_4$

$\Rightarrow V_o = (2V_1 + 4V_3) - (3V_2 + 5V_4)$

$\boxed{V_o = V_{o1} - V_{o2}} \rightarrow (1)$ where $V_{o1} = 2V_1 + 4V_3$

$V_{o2} = 3V_2 + 5V_4$

Eqn (1) is the expression for output voltage of subtractor.

Consider

$V_{o1} = 2V_1 + 4V_3$

Comparing with,

$V_{o1} = \frac{R_{f1}}{R_1} V_1 + \frac{R_{f1}}{R_3} V_3$

$\Rightarrow \frac{R_{f1}}{R_1} = 2, \quad \frac{R_{f1}}{R_3} = 4$

Let $R_{f1} = 100\,k\Omega$.

$\therefore R_1 = 50\,k\Omega, \quad R_3 = 25\,k\Omega$

Consider

$V_{o2} = 3V_2 + 5V_4$, Comparing with

$V_{o2} = \frac{R_{f2}}{R_2} V_2 + \frac{R_{f2}}{R_4} V_4$

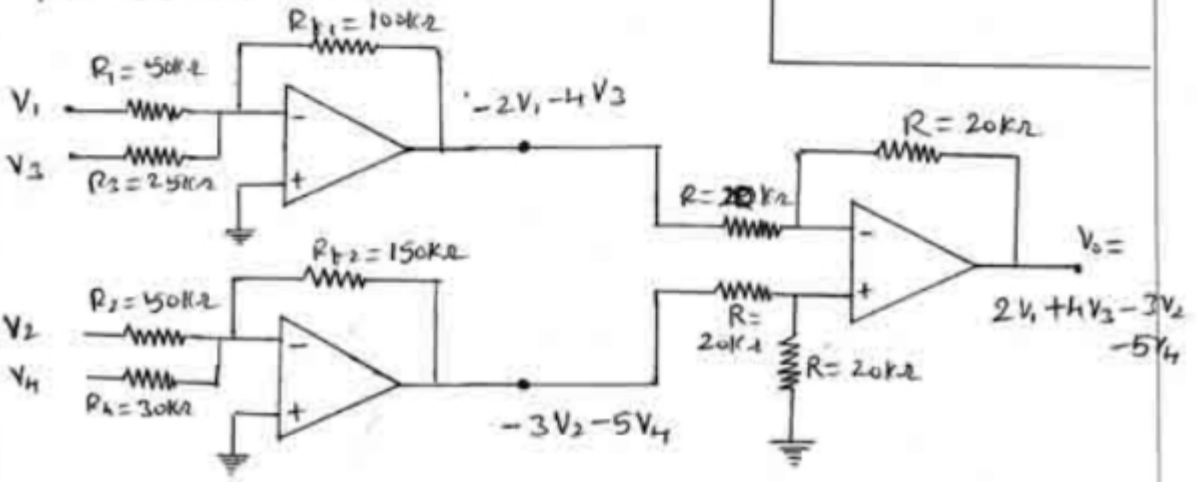
$\Rightarrow \frac{R_{f2}}{R_2} = 3, \quad \frac{R_{f2}}{R_4} = 5$

Let $R_{f2} = 150\,k\Omega$

$\therefore R_2 = 50k\Omega, \quad R_4 = 30k\Omega$

The op-amp circuit is shown below

Let $R = 20k\Omega$



MODULE-3: DIGITAL ELECTRONICS

Syllabus: Introduction, Switching and logic levels, Digital Waveform. Number Systems: Decimal number System, Binary number System, Converting Decimal to Binary, Hexadecimal Number System, Converting Binary to Hexadecimal, Hexadecimal to Binary, Converting Hexadecimal to Decimal, Converting Decimal to Hexa-decimal, Octal numbers: Binary to octal conversion, Complement of Binary Numbers, Boolean algebra theorem, De morgan's theorem, Digital Circuits: logic gates, NOT Gate, AND gate, OR gate, XOR gate, NAND gate, NOR gate, X-NOR gate, Algebraic Simplification, NAND & NOR implementation: NAND implementation, NOR implementation, Half adder, Full adder.

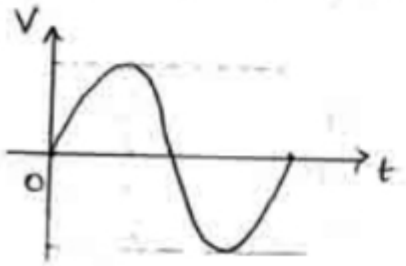
* Introduction:

→ A continuously varying signal (Voltage or current) is called an analog signal

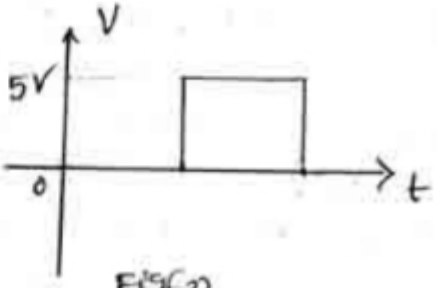
Ex: Sinusoidal voltage (fig 1)

→ A signal (Voltage or current) which is having only two discrete values is called a digital signal

Ex: Square wave (fig 2)



Fig(1)



Fig(2)

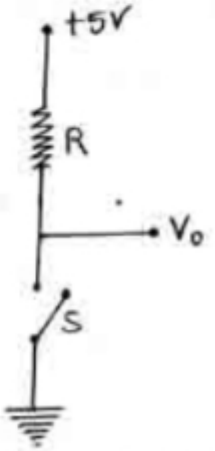
Analog domain	Digital domain
① An analog signal can have infinite number of values	① A Digital signal can have only two values (5V & 0V) These values are, high (ON/1) & low (OFF) (0)
② Analog systems are generally difficult to design	② Digital systems are generally easier to design.
③ Information storage is difficult	③ Information storage is easy
④ Accuracy & precision are less	④ Accuracy & precision are greater
⑤ Operation cannot be Progra-rmed	⑤ operation can be Programmed
⑥ Analog circuits are affected by noise	⑥ Digital circuits are less affected by noise
⑦ Analog signals consume less bandwidth (BW)	⑦ Digital signals consume more BW.
⑧ Analog circuits are constru-cted using R, L, C & op-amp etc	⑧ Digital circuits are constructed using adders, multipliers, memory etc

* Switching and Logic levels:

The switching circuit is shown in fig③.

When the switch 'S' is open ⑤ OFF ⑥ False ⑦ NO ⑧ Low, the output voltage is $V_o = 5V$ ⑨ ON ⑩ High ⑪ True ⑫ Yes.

When the switch 'S' is closed ⑬ ON ⑭ True ⑮ Yes, the output $V_o = 0V$ ⑯ Low ⑰ OFF ⑱ False.



Fig③ : Switching circuit

Therefore input '0' results in output '1' & vice versa & hence this circuit is called as switching circuit (or) state inversion circuit (or) inverter (or) NOT gate.

NOT gate symbol is shown in fig (4)

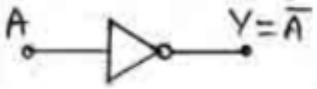


Fig (4)

A	Y
0	1
1	0

Fig (5)

Fig (5) shows the truth table (input-output relationship) of NOT gate

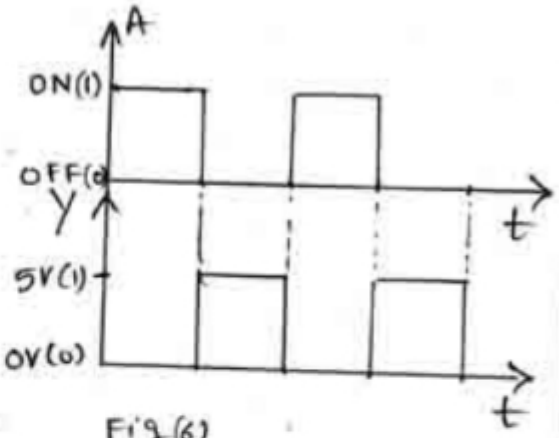


Fig (6)

Fig (6) shows the input-output waveforms of NOT gate.

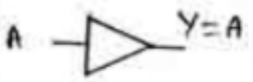
Note:

(0 & 1s)

(1) The branch of electronics which deals with digital circuits is called digital electronics.

(2) An electronic circuit that handles only a digital signal (Low (or) high) is called a digital circuit

(3) Buffer: (Non inverter)



Buffer symbol

A	Y
0	0
1	1

Buffer truth table

(4) Types of Number systems (digital number systems)

(a) Decimal Ex: $(15)_{10}$ (or) 15_{10} (uses 0 to 9)

⑥ Binary Ex: $(101)_2$ @ 101_2 (Uses 0 and 1)

© Octal Ex: $(37)_8$ @ 37_8 (Uses 0 to 7)

② Hexadecimal Ex: $(3AC)_{16}$ @ $3AC_{16}$ (Uses 0 to 9 & A, B, C, D, E, F)

etc

⑤ Each binary digit (0 @ 1) is bit

A string of four bits is nibble (1010)

A string of eight bits is byte. (1010 0110)

⑥ Digital circuits which accomplishes (Performs) some operation (Boolean algebra) are logic gates

⑦ Branch of algebra which deals with only 0's & 1's is called Boolean algebra. @ (Algebra used to symbolically describe logic functions)

---

* Digital Waveform:

Ideally:

High = 5V = 1

Low = 0V = 0

Practically:

Voltages at different points may slightly vary (due to internal resistances, parasitic effects & loading effects)

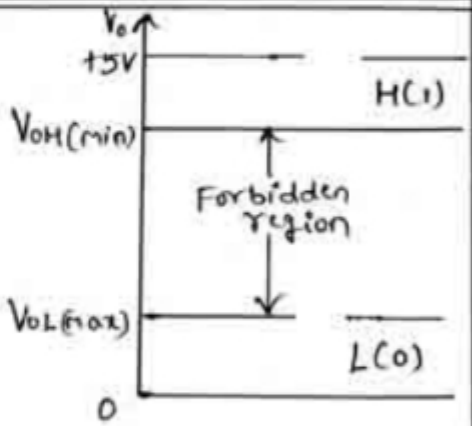


Fig ⑦ : Voltage ranges for logic levels

∴ High voltage = Voltage between +5V & $V_{OH(min)}$ (Ex: 5V to 3.5V)

Low voltage = Voltage between 0V & $V_{OL(max)}$ (Ex: 0V to 0.2V)

Forbidden region = $V_{OH(min)} - V_{OL(max)}$ (Ex: 3.5 − 0.2 = 3.3V)

[Neither H(1) @ L(0)]

* **Number Systems:**

There are four number systems that are used in digital systems:

1). Decimal 2). Binary 3). Octal 4) Hexadecimal.

①. Decimal number system

→ Decimal number system uses the digits 0 to 9 (10)

→ Any number N in a positional number system or radix-weighted positional number system is represented by.

$$N = d_{n-1}\, d_{n-2} \ldots d_1 d_0 . d_{-1} \ldots d_{-m} \quad \text{— ①}$$

$$= d_{n-1} \times r^{n-1} + d_{n-2} \times r^{n-2} + \cdots + d_0 \times r^0 + d_{-1} \times r^{-1} + \cdots + d_{-m} \times r^{-m} \quad \text{— ②}$$

where, d_i → Digit in the number system $[0 \le d_i \le (r-1)]$

r → base or radix of the number system.

n → number of digits in the integer part of N.

m → number of digits in the fraction part of N.

Ex: $2438 = 2000 + 400 + 30 + 8$

$= 2 \times 10^3 + 4 \times 10^2 + 3 \times 10^1 + 8 \times 10^0$

$N = 2438$, $d_{n-1} = 2$, $d_{n-2} = 4$, $d_0 = 8$, $r = 10$, $n = 4$

②. Binary number system

→ Binary number system uses the digits 0 & 1 (2)

→ Ex: $1101 = 1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$ — ③

$= 8 + 4 + 0 + 1$

$= 13_{10}$

Comparing ② & ③, we can write $d_3 = 1, d_2 = 1, d_1 = 0, d_0 = 1$

$N = 1101$, $r = 2$, $n = 4$.

③ Octal number System

→ Octal number System uses the digits 0 to 7 (8)

→ Ex: $43672 = 4\times8^4 + 3\times8^3 + 6\times8^2 + 7\times8^1 + 2\times8^0$ —④

$= 16384 + 1536 + 384 + 56 + 2$

$= 18362_{10}$

Comparing ② & ④, we can write,

$d_4 = 4$, $d_3 = 3$, $d_2 = 6$, $d_1 = 7$, $d_0 = 2$, $n = 5$, $r = 8$

$N = 43672$

④ Hexadecimal number System

→ Hexadecimal number System uses the digits 0 to 9 & A, B, C, D, E, F (16)

→ Ex: $AB3 = 10\times16^2 + 11\times16^1 + 3\times16^0$ —⑤

$= 2560 + 176 + 3$

$= 2739_{10}$

Comparing ② & ⑤, we can write

$d_2 = A = 10$, $d_1 = B = 11$, $d_0 = 3$, $n = 3$, $r = 16$, $N = AB3$

* Conversions:

① Decimal to Binary:

⑨ Convert the decimal number 109 to binary

Sol:

2 | 109	
2 | 54	– 1
2 | 27	– 0
2 | 13	– 1
2 | 6	– 1
2 | 3	– 0
1	– 1

$\therefore (109)_{10} = (1101101)_2$ //

(b) Perform the following:

(i) $(69)_{10} = (?)_2$ (ii) $53.75_{10} = ?_2$ (iii) $0.375_{10} = ?_2$

Sol:

(i)

2 | 69	
2 | 34	-1
2 | 17	-0
2 | 8	-1
2 | 4	-0
2 | 2	-0
	1 -0

$\therefore \boxed{(69)_{10} = (1000101)_2}$

(ii) Consider (Whole) Integer Part

2 | 53	
2 | 26	-1
2 | 13	-0
2 | 6	-1
2 | 3	-0
	1 -1

$\therefore (53)_{10} = (110101)_2$

Consider fractional Part

	Integer
$0.75 \times 2 = 1.5$	1
$0.5 \times 2 = 1$	1

$\therefore 0.75_{10} = 0.11_2$

$\therefore \boxed{(53.75)_{10} = (110101.11)_2}$ //.

(iii)

	Integer
$0.375 \times 2 = 0.75$	0
$0.75 \times 2 = 1.5$	1
$0.5 \times 2 = 1$	1

$\therefore \boxed{0.375_{10} = 0.011_2}$ //.

(2) Binary to Decimal:

(a) Convert the following binary numbers to decimal numbers.

(i) 1101 (ii) 10001.11 (iii) 0.1011

Sol:

(i) $1101 = 1\times2^3 + 1\times2^2 + 0\times2^1 + 1\times2^0 = 8+4+1 = (13)_{10}$

(ii) $10001.11 = 1\times2^4 + 1\times2^0 + 1\times2^{-1} + 1\times2^{-2} = 16 + 1 + 0.5 + 0.25$
$= (17.75)_{10}$ //.

(iii) $0.1011 = 1\times2^{-1} + 1\times2^{-3} + 1\times2^{-4} = 0.5 + 0.125 + 0.0625$
$= (0.6875)_{10}$ //.

④ Perform the following (i) $(0.1011)_2 = (?)_{10}$

Sol:

$0.1011 = 1\times2^{-1} + 0\times2^{-2} + 1\times2^{-3} + 1\times2^{-4}$

$= 0.5 + 0 + 0.125 + 0.0625$

$\boxed{(0.1011)_2 = (0.6875)_{10}}$ //.

③ Decimal to octal:

② Convert the following decimal numbers to octal numbers

(i) 359 (ii) 658.825 (iii) 0.245 (iv) 254

Sol:

(i)

8	359	
8	44	−7 ↑
	5	−4

$\therefore \boxed{(359)_{10} = (547)_8}$ //

(ii) Consider integer Part (Whole no)

8	658	
8	82	−2 ↑
8	10	−2
	1	−2

$\therefore (658)_{10} = (1222)_8$

Consider fractional Part

	Integer
$0.825\times8 = 6.6$	6
$0.6\times8 = 4.8$	4
$0.8\times8 = 6.4$	6
$0.4\times8 = 3.2$	3 ↓

$\therefore 0.825_{10} = 0.6463_8$

$\therefore \boxed{(658.825)_{10} = (1222.6463)_8}$ //

(iii)

	Integer
$0.245\times8 = 1.96$	1
$0.96\times8 = 7.68$	7
$0.68\times8 = 5.44$	5
$0.44\times8 = 3.52$	3 ↓

$\therefore \boxed{(0.245)_{10} = (0.1753)_8}$

(iv)

8	254	
8	31	−6 ↑
	3	−7

$\therefore \boxed{(254)_{10} = (376)_8}$ //

⑤ Perform the following upto 2 octal Places

$(0.44)_{10} = ?_8$

Sol:

	Integer
$0.44 \times 8 = 3.52$	3 ↓
$0.52 \times 8 = 4.16$	4 ↓

$\therefore \boxed{(0.44)_{10} = 0.34_8}$ //.

(4) Octal to Decimal:

(a) Perform the following

(i) $(133)_8 = (?)_{10}$ (ii) $372_8 = ?_{10}$ (iii) $24.6_8 = ?_{10}$

(iv) $0.76_8 = ?_{10}$

Sol:

(i) $\overset{2}{1}\overset{1}{3}\overset{0}{3}_8 = 1\times8^2 + 3\times8^1 + 3\times8^0 = 64 + 24 + 3 = 91_{10}$ //.

(ii) $\overset{2}{3}\overset{1}{7}\overset{0}{2}_8 = 3\times8^2 + 7\times8^1 + 2\times8^0 = 192 + 56 + 2 = 250_{10}$ //.

(iii) $\overset{1}{2}\overset{0}{4}.\overset{-1}{6}_8 = 2\times8^{+1} + 4\times8^0 + 6\times8^{-1} = 16 + 4 + 0.75 = 20.75_{10}$ //.

(iv) $0.\overset{-1}{7}\overset{-2}{6}_8 = 7\times8^{-1} + 6\times8^{-2} = 0.875 + 0.09375 = 0.96875_{10}$

(b) Convert the following octal number to decimal number

(i) 564 (ii) 234.56

Sol:

(i) $\overset{2}{5}\overset{1}{6}\overset{0}{4}_8 = 5\times8^2 + 6\times8^1 + 4\times8^0 = 320 + 48 + 4 = 372_{10}$ //.

(ii) $\overset{2}{2}\overset{1}{3}\overset{0}{4}.\overset{-1}{5}\overset{-2}{6}_8 = 2\times8^2 + 3\times8^1 + 4\times8^0 + 5\times8^{-1} + 6\times8^{-2}$

$= 128 + 24 + 4 + 0.625 + 0.09375$

$= 156.71875_{10}$

(5) Decimal to Hexadecimal

(a) Perform the following

(i) $(541)_{10} = (?)_{16}$ (ii) $378_{10} = ?_{16}$

Sol:

(i)
16 | 541
16 | 33 – 13 (D)
2 – 1

$\therefore (541)_{10} = (21D)_{16}$

(ii)
16 | 378
16 | 23 – 10(A)
1 – 7

$\therefore 378_{10} = 17A_{16}$

(5) convert the following decimal numbers to Hexadecimal numbers.

(i) 5386.345 (ii) 0.256 upto 3 Hexadecimal places

Sol:

(i) (Whole number)

Consider integer Part

16 | 5386
16 | 336 – 10 (A)
16 | 21 – 0
1 – 5

$\therefore 5386_{10} = 150A_{16}$

Consider fractional Part

	Integer
$0.345 \times 16 = 5.52$	5
$0.52 \times 16 = 8.32$	8
$0.32 \times 16 = 5.12$	5
$0.12 \times 16 = 1.92$	1

$\therefore 0.345_{10} = 0.5851_{16}$

$\therefore (5386.345)_{10} = (150A.585)_{16}$ //.

(ii)

	Integer
$0.256 \times 16 = 4.096$	4
$0.096 \times 16 = 1.536$	1
$0.536 \times 16 = 8.576$	8

$\therefore 0.256_{10} = 0.418_{16}$ //.

(6) Hexadecimal to decimal

(a) Perform the following

(i) $(FACE)_{16} = (\ ?\ )_{10}$ (ii) $(AB.32)_{16} = (?)_{10}$

Sol:

(i) $(\overset{3}{F}\overset{2}{A}\overset{1}{C}\overset{0}{E})_{16} = F\times16^3 + A\times16^2 + C\times16^1 + E\times16^0$

$= 15\times16^3 + 10\times16^2 + 12\times16 + 14\times1$

$= 61440 + 2560 + 192 + 14$

$\boxed{(FACE)_{16} = (64206)_{10}}$ //.

(ii) $(\overset{1}{A}\overset{0}{B}.\overset{-1}{3}\overset{-2}{2})_{16} = A\times16^1 + B\times16^0 + 3\times16^{-1} + 2\times16^{-2}$

$= 10\times16 + 11\times1 + \frac{3}{16} + \frac{2}{16^2}$

$= 160 + 11 + 0.1875 + 0.0078125$

$\boxed{(AB.32)_{16} = (171.1953125)_{10}}$

(b) Convert the following hexadecimal number to decimal number.

(i) 3AB4.12 (ii) ABCDE

Sol: $3\overset{3}{A}\overset{2}{B}\overset{1}{4}.\overset{-1}{1}\overset{-2}{2} = 3\times16^3 + A\times16^2 + B\times16^1 + 4\times16^0 + 1\times16^{-1} + 2\times16^{-2}$

$= 3\times16^3 + 10\times16^2 + 11\times16 + 4\times1 + \frac{1}{16} + \frac{2}{16^2}$

$= 12288 + 2560 + 176 + 4 + 0.0625 + 0.0078125$

$\boxed{3AB4.12_{16} = 15028.07031_{10}}$ //.

(ii) $\overset{4}{A}\overset{3}{B}\overset{2}{C}\overset{1}{D}\overset{0}{E}_{16} = A\times16^4 + B\times16^3 + C\times16^2 + D\times16^1 + E\times16^0$

$= 10\times16^4 + 11\times16^3 + 12\times16^2 + 13\times16 + 14\times1$

$= 655360 + 45056 + 3072 + 208 + 14$

$\boxed{ABCDE_{16} = 703710_{10}}$ //.

Note:

① What is the largest number that can be represented using eight bits?

Sol: $N = 8$

Largest number $= 2^N - 1 = 2^8 - 1 = 255_{10} = 11111111_2$

② Determine the value of base x, if

(i) $(225)_x = (341)_8$ (ii) $(211)_x = (152)_8$

Sol:

(i) Given

$(225)_x = (341)_8$ — ①

Convert $(341)_8$ to decimal

$(\overset{2}{3}\overset{1}{4}\overset{0}{1})_8 = 3\times8^2 + 4\times8^1 + 1\times8^0$

$= 192 + 32 + 1$

$(341)_8 = (225)_{10}$ — ②

From ① & ②, we get

$\boxed{x = 10}$

(ii) Given

$(211)_x = (152)_8$

Convert $(152)_8$ to decimal

$(\overset{2}{1}\overset{1}{5}\overset{0}{2})_8 = 1\times8^2 + 5\times8^1 + 2\times8^0$

$= 64 + 40 + 2$

$(152)_8 = (106)_{10}$ — ①

$\therefore (\overset{2}{2}\overset{1}{1}\overset{0}{1})_x = 2\times x^2 + 1\times x + 1\times x^0$

$(211)_x = 2x^2 + x + 1$ — ②

From ① & ②, we get

$2x^2 + x + 1 = 106$

$\Rightarrow 2x^2 + x - 105 = 0$

$x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$ $\quad a=2,\ b=1,\ c=-105$

$= \frac{-1 \pm \sqrt{1^2 + 4\times2\times105}}{2\times2}$

$= \frac{-1 \pm 29}{4}$

$= 7$ or -7.5

$\therefore \boxed{x = 7}$

③ Octal - binary number

Octal number	Binary Equivalent
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Table ①

④ To write any number in binary we use

2^4 2^3 2^2 2^1 2^0 (Using 5 bits)
(16) (8) (4) (2) (1)

Ex:

$10 = 8+2 \rightarrow 01010$

$14 = 8+4+2 \rightarrow 01110$

⑤ Hexadecimal - binary - decimal

Decimal number	Hexadecimal number	Binary Equivalent
0	0	0000
1	1	0001
2	2	0010
3	3	0011
4	4	0100
5	5	0101
6	6	0110
7	7	0111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

Table ②

Extra numerical:

① convert octal 143 to binary

Sol: $143_8 = (001\ 100\ 011)_2$ [From table ①]

② Perform the following

(i) $(232.76)_8 = (?)_2$ (ii) $(43.26)_8 = ?_2$

Sol: (i) $232.76_8 = (010\ 011\ 010 . 111\ 110)_2$ //

(ii) $\boxed{43.26_8 = (100\,011 . 010\,110)_2}$ //..

(3) Perform the following

(i) $(110101)_2 = (?)_8$ (ii) $(10100)_2 = (?)_8$

(iii) $(1101001.1101)_2 = ?_8$

Sol:

(i) $\underbrace{110}_{6}\ \underbrace{101}_{5}$ $\therefore \boxed{(10101)_2 = (65)_8}$ //

(ii) $(10100)_2 = \underbrace{010}_{2}\ \underbrace{100}_{4} = (24)_8$

(iii) $1101001.1101 = \underbrace{001}\ \underbrace{101}\ \underbrace{001} . \underbrace{110}\ \underbrace{100} = (151.64)_8$

(4) Perform the following

(i) $FAFB_{16} = ?_2$ (ii) $(A3.D24)_{16} = (?)_2$

Sol:

(i) $FAFB_{16} = \underbrace{1111}_{F(15)}\ \underbrace{1010}_{A(10)}\ \underbrace{1111}_{F(15)}\ \underbrace{1011}_{B(11)}$

$\therefore \boxed{FAFB_{16} = 1111101011111011_2}$ //..

(ii) $(A3.D24)_{16} = \underbrace{1010}_{A(10)}\ \underbrace{0011}_{3} . \underbrace{1101}_{D(13)}\ \underbrace{0010}_{2}\ \underbrace{0100}_{4}$

$\therefore \boxed{(A3.D24)_{16} = (10100011.110100100100)_2}$ //.

(5) Perform the following

(i) $(4567)_{10} = (?)_2 = (?)_8 = (?)_{16}$

Sol: (ii) $(101101110.11011)_2 = (?)_{16}$

(i)

2 | 4567	
2 | 2283 - 1	
2 | 1141 - 1	
2 | 570 - 1	
2 | 285 - 0	
2 | 142 - 1	
2 | 71 - 0	
2 | 35 - 1	
2 | 17 - 1	
2 | 8 - 1	
2 | 4 - 0	
2 | 2 - 0	
1 - 0	

$\therefore (4567)_{10} = (1000111010111)_2$

$0001\ 0001\ 1101\ 0111$

1 0 7 2 7

$\therefore (1000111010111)_2 = (10727)_8$

$0001\ 0001\ 1101\ 0111$

1 1 D 7

$\therefore (1000111010111)_2 = (11D7)_{16}$

$\therefore \boxed{(4567)_{10} = (1000111010111)_2 = (10727)_8 = (11D7)_{16}}$ //.

(ii)

$0001\ 0110\ 1110.1101\ 1000$

1 6 E . D 8

$\therefore \boxed{(10110111 0.11011)_2 = (16E.D8)_{16}}$ //.

* Binary addition : [0 & 1]

Rules

① 0 + 0 = 0 (Sum), 0 (Carry)

② 0 + 1 = 1 (Sum), 0 (Carry)

③ 1 + 0 = 1 (Sum), 0 (Carry)

④ 1 + 1 = 0 (Sum), 1 (Carry)

1 + 1 = 2

2 \| 2

1 - 0

Carry, Sum

⑤
```
  1
  1
 +1
 --
 11
 ↑↑
carry sum
```

```
  1
  1
 +1
 --
  3
```

```
2|3
 1 -1
 ↑  ↑
carry sum
```

Q Add the following binary numbers

ⓐ 11011 & 10111 ⓑ 101 & 011 ⓒ 11.01 & 10.11

Sol:

ⓐ
```
  11011
+ 10111
---------
(110010)2
```

ⓑ
```
  101
+ 011
-------
(1000)2
```

ⓒ
```
  11.01
+ 10.11
---------
(110.00)2
```

* Octal & hexadecimal addition: [(0-7 for octal) & (0-9 & A-F for Hexa)]

Q Perform the following

(i) $(43.26)_8 + (31.42)_8 = (\ ?\ )_8$

(ii) $(ABCD)_{16} + (AB32)_{16} = (\ ?\ )_{16}$

Sol:

(i)
```
  1
 43.26
+31.42
--------
(74.70)8
```

```
 6
 2
8 8|8
   1-0
```

(ii)
```
    1
 ABCD
+AB32
---------
(156FF)16
```

```
 B
 B
 22
16|22
  1-6
16|21
  1-5
```

* Binary subtraction:

Rules

① 0 − 0 = 0 (Borrow 0, difference 0)

② 0 − 1 = 1 (Borrow 1, difference 1)

③ 1 − 0 = 1 (Borrow 0, difference 1)

④ 1 − 1 = 0 (Borrow 0, difference 0)

① Perform the following binary subtraction

ⓐ 1101 − 1000 ⓑ 1000 − 1101

Sol:

ⓐ
$$\begin{array}{r} 1101 \\ -1000 \\ \hline 0\ (0101)_2 \end{array}$$
↑ Borrow

Borrow = 0, Answer is +ve

In decimal: 13 − 8 = 5

ⓑ
$$\begin{array}{r} 1000 \\ -1101 \\ \hline (1)\ 1011 \end{array}$$
Borrow

1's complement of 1011 → 0100 + 1

$$-(0101)_2$$

Borrow = 1, Answer is −ve & 1's complement of result & add Borrow give result

In decimal: 8 − 13 = −5

* Complement of Binary numbers:

① Write the 1's complement and 2's complement of the following ⓐ 10101 ⓑ 11100.101 ⓒ 11100

Sol:

ⓐ Given 10101

1's complement of 10101 → 01010

2's complement of 10101 → 01011

1's complement of 10101 → 01010 + 1

2's complement of 10101 → 01011

ⓑ Given 11100.101

1's complement of 11100.101 → 00011.010

2's complement of 11100.101 → 00011.010 + 1 = 00011.011

ⓒ Given 11100

00011 → 1's complement of 11100

+ 1

00100 → 2's complement of 11100

② Perform the following binary Subtraction using
ⓐ 1's Complement ⓑ 2's Complement
(i) 1110 − 1001 (ii) 1001 − 1110

Sol:

ⓐ 1's Complement

(i) 1110 → Minuend
−1001 → Subtrahend

1110 → Minuend
+0110 → 1's complement of Subtrahend (1001)

10100
Carry → 1 +

(0101)$_2$

(ii) 1001 → Minuend
− 1110 → Subtrahend

1001 → Minuend
+ 0001 → 1's Complement of Subtrahend (1110)

1010
↗ No Carry

Take 1's Complement of 1010

∴ −(0101)$_2$

No Carry, −Ve, Take 1's Complement
Carry, +Ve, Add Carry to result

ⓑ 2's Complement

(i) 1110 → Minuend
−1001 → Subtrahend

1110 → Minuend
+0111 → 2's Complement of 1001 (Subtrahend)

(1)(0101)$_2$
↑ Carry (Discard)

(ii) 1001 → Minuend
−1110 → Subtrahend

1001 → Minuend
+0010 → 2's Complement of Subtrahend (1110)

1011
↑ No Carry

∴ Take 2's Complement of 1011

∴ −(0101)$_2$

No Carry, result is −Ve

In decimal (i) 14 − 9 = 5 (ii) 9 − 14 = −5

③ Perform the following binary subtraction using 1's complement and 2's complement

ⓐ 1111 − 1101 ⓑ 10111 − 10101

Sol:

1's Complement

ⓐ 1111 → Minuend
− 1101 → Subtrahend

1111 → Minuend
+ 0010 → 1's complement of Subtrahend (1101)

① 0001
Carry → 1 +

$(0010)_2$

ⓑ 10111 → Minuend
− 10101 → Subtrahend

10111 → Minuend
+ 01010 → 1's complement of Subtrahend (10101)

① 00001
Carry → 1 +

$(00010)_2$

2's Complement

ⓐ 1111 → Minuend
− 1101 → Subtrahend

1111 → Minuend
+ 0011 → 2's complement of Subtrahend (1101)

① 0010

Carry
Discard

ⓑ 10111 → Minuend
− 10101 → Subtrahend

10111 → Minuend
+ 01011 → 2's complement of Subtrahend (10101)

① $(00010)_2$

Carry
Discard

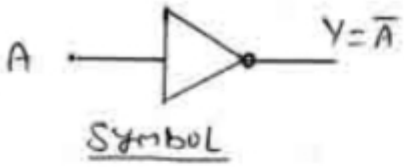
* Logic gates

① NOT gate (or) (Inverter) (or) (Complementor): $(-)^{@}(')$

*The output is the reverse of the input. ie a low-voltage input (0) is converted to a high-voltage output (1) & vice versa.

* If 'A' is the input, then output, $Y = \bar{A}$

*The Symbol & truth table of a NOT gate is shown in fig ①.



Symbol

A	Y=Ā
0	1
1	0

Truth table

Fig ①

*The input and output waveforms of a NOT gate is shown in fig ②

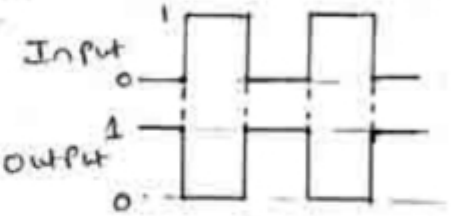


Fig ②

* The circuit diagram of a transistor based NOT gate is shown in fig ③

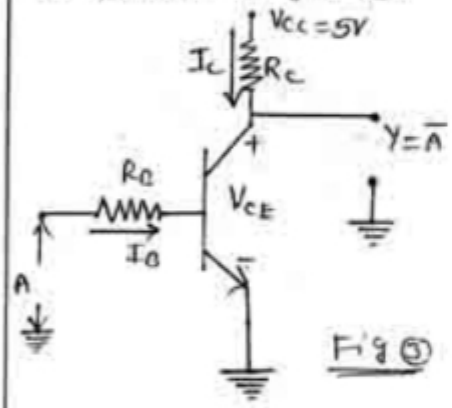


Fig ③

→ When A = 5V, Y = 0V

→ When A = 0V, Y = 5V

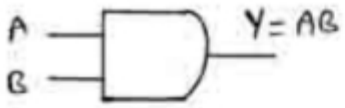
② AND gate: (.)

* The output is 1 only if both A and B are 1, otherwise it is zero.

* If A and B are the inputs, then the output of AND gate is.

$Y = A.B$ or AB

* The Symbol & truth table of AND gate is shown in fig ④



Symbol

Fig ④

A	B	Y=AB
0	0	0
0	1	0
1	0	0
1	1	1

Truth table

* The input & output waveforms of a AND gate is shown in fig ⑤

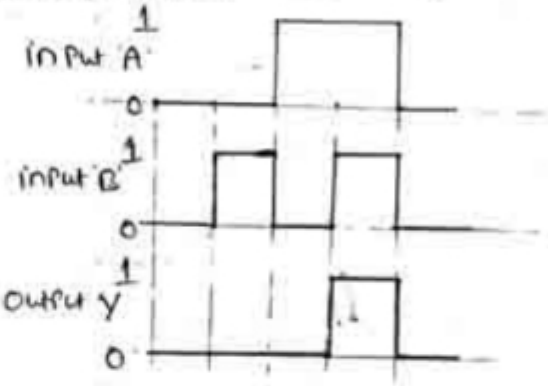


Fig ⑤

* The circuit diagram of an AND gate using diodes is shown in fig ⑥.

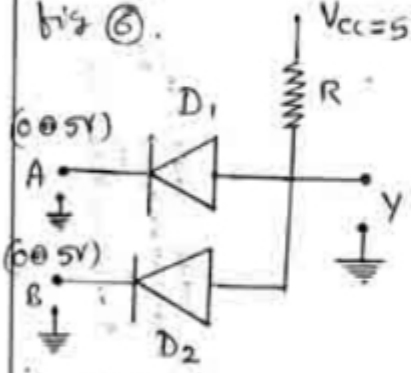


Fig ⑥

* If A = B = 5V, the diodes D1 & D2 doesn't conduct (Open circuit), then the output Y = 5V
* If atleast one input (A ⊕ B) is 0V, then the output Y = 0V.

Note:

① Consider the simple electric circuit shown in fig ⑦

A, B → Switches (Closed = 1, Open = 0)

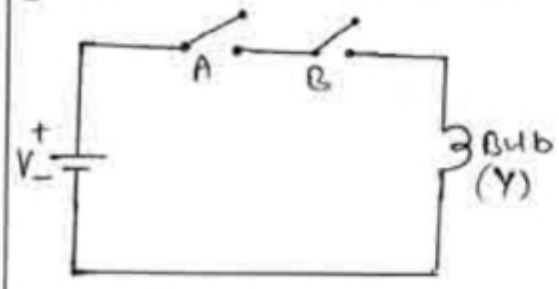


Fig ⑦

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

② AND gate with N inputs (output is 1 only when all the inputs are 1)

$Y = A.B.C.\ldots.N$

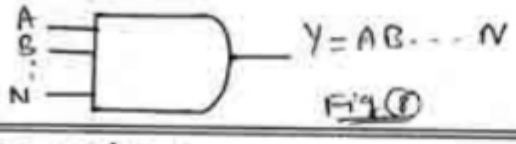


Fig ⑧

③ NAND-gate is the dual of NOR-gate & vice versa

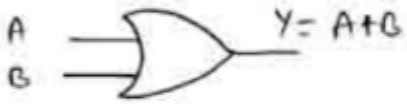
---

③ OR gate(+):

* The output is 0 when all the inputs are zero, otherwise it is 1.
* If A and B are the inputs, then the output of OR gate is,

$Y = A + B.$

* The symbol & truth table of OR gate is shown in fig ⑨.



Symbol

Fig ⑨

A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

Truth table

* The input and output waveforms of a OR gate is shown in fig ⑩.
* The circuit diagram of an OR gate using diodes is shown in fig ⑪

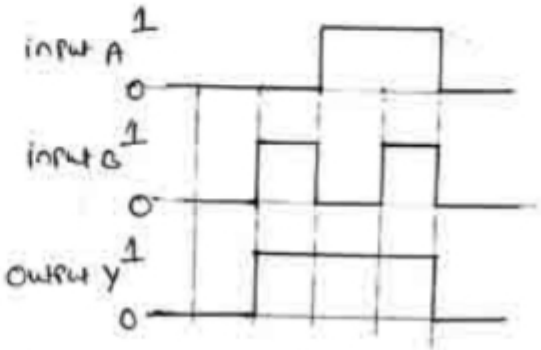


Fig ⑩

* When A=B=0V, the diodes D_1 & D_2 doesnot conduct, hence the output Y=0V.

* When either A & B (or) both are at 5V(1), the diodes D_1 & D_2 are on (Conducts) hence the output Y = 1V

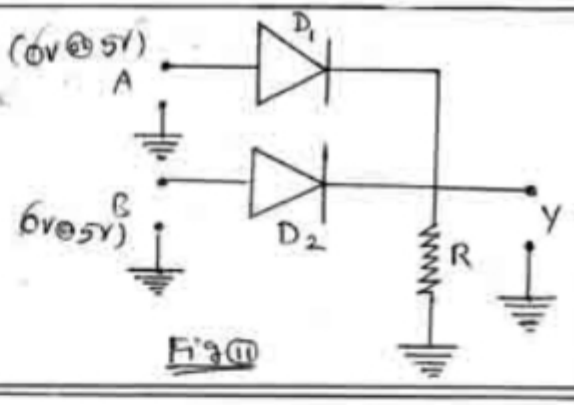


Fig (11)

Note:

(1) Consider the simple electric circuit shown in fig (12)

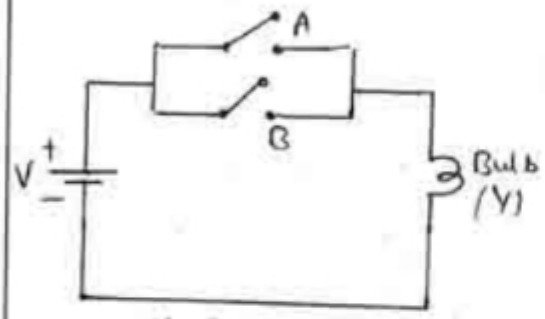


Fig (12)

A, B → Switches (Closed = 1, Open = 0)

A	B	y
0	0	0
0	1	1
1	0	1
1	1	1

(2) OR gate with N inputs (Output is '0' when all the inputs are '0')

$Y = A + B + C + \dots + N$

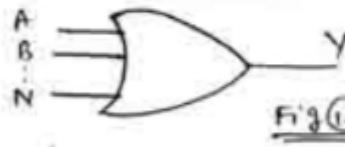


Fig (13)

(3) $\bar{0} = 1$

(4) $\bar{1} = 0$

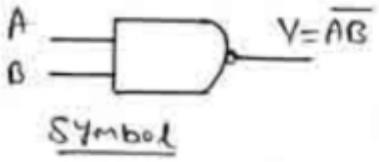
(4) NAND gate:

* The output is '0' (Low) only if both A & B are 1, otherwise it is 1.

* If A and B are the inputs, then the output of NAND gate is,

$$Y = \overline{AB}$$

* The Symbol & truth table of NAND gate is shown in fig (14)



Symbol

Fig (14)

A	B	Y= $\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

Truth table

* The input & output waveforms of NAND gate is shown in fig (15)

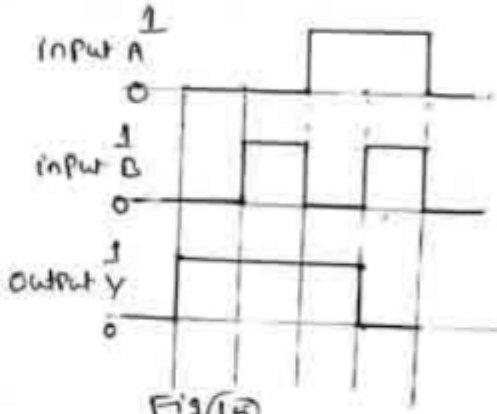


Fig (15)

* The output 'Y' of 'N' inputs NAND gate is,

$$Y = \overline{ABC\ldots N}$$

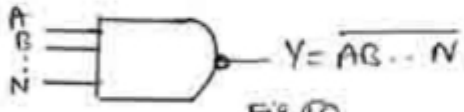


Fig (16)

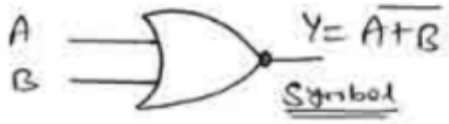
(5) NOR gate:

* The output is '1' (high) when all the inputs are '0' (LOW), otherwise it is '0' (LOW)

* If A and B are the inputs, then the output of NOR gate is,

$$Y = \overline{A+B}$$

* The Symbol & truth table of NOR gate is shown in fig (17)



Symbol

Fig (17)

A	B	Y= $\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Truth table

* The input and output waveforms of NOR gate is shown in fig (18).

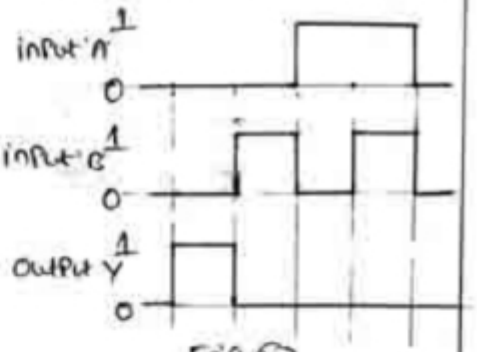


Fig (18)

* The output of 'N' inputs NOR gate is,

$$Y = \overline{A+B+\cdots+N}$$

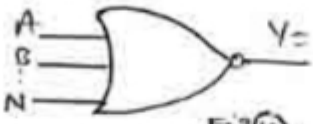


Fig (19)

(6) EXOR gate @ Exclusive-OR gate:

* The output is '1' (high), when the inputs are different, otherwise it is '0' (LOW)

Symbol

* If A and B are the inputs, then the output of XOR gate is,

$$Y = A \oplus B = \bar{A}B + A\bar{B} \left(= \overline{\bar{A}\bar{B} + AB}\right)$$

* The Symbol & truth table of XOR gate is shown in fig (20)

A	B	Y = A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

Truth table

Fig (20)

* The input & output waveforms of XOR gate is shown in fig (21)

* The output of 'N' inputs XOR gate is, (output is 1 when odd number of inputs are high)

$$Y = A \oplus B \oplus \cdots \oplus N$$

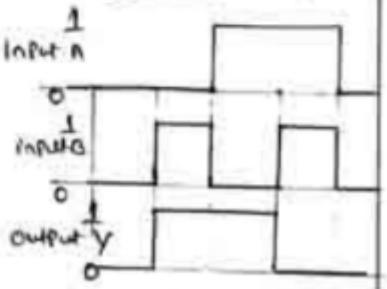


Fig (21)

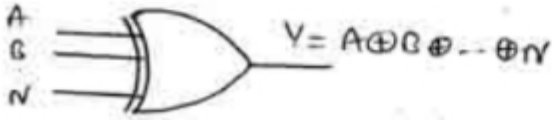
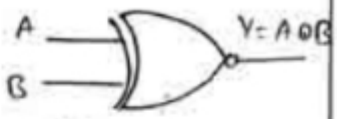


Fig (22)

⑦ EX-NOR gate @ Exclusive-NOR gate

* The output is '1' (high) when both inputs are same [(0,0) @ (1,1)].



Symbol

* If A and B are the inputs, then the output of EX-NOR gate is,

$$Y = A \odot B = \bar{A}\bar{B} + AB \; (= \bar{A}B + A\bar{B})$$

* The symbol & truth table of EX-NOR gate is shown in fig (23)

A	B	Y = A⊙B
0	0	1
0	1	0
1	0	0
1	1	1

Truth table

Fig (23)

* The output 'Y' of N inputs EX-NOR gate is (output is high only when even number of ones @ all inputs are high)

$$Y = A \odot B \odot \ldots \odot N$$

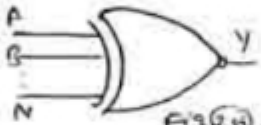


Fig (24)

* The input & output waveforms of EX-NOR gate is shown in fig (24)

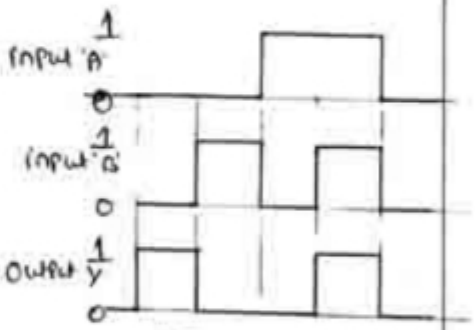


Fig (24)

* Boolean algebra theorems @ (Basic Boolean Laws):

Name	AND form	OR form
Identity Law	$1 \cdot A = A$	$0 + A = A$
Null Law	$0 \cdot A = 0$	$1 + A = 1$
Idempotent Law	$A \cdot A = A$	$A + A = A$
Inverse Law	$A \cdot \bar{A} = 0$	$A + \bar{A} = 1$
Commutative Law	$AB = BA$	$A + B = B + A$
Associative Law	$(AB)C = A(BC)$	$(A+B)+C = A+(B+C)$
Distributive Law	$A+BC = (A+B)(A+C)$	$A(B+C) = AB+AC$
Absorption law	$A(A+B) = A$	$A+AB = A$
DeMorgan's Law	$\overline{A \cdot B} = \bar{A} + \bar{B}$	$\overline{A+B} = \bar{A} \cdot \bar{B}$

Absorption Law is also called as Redundance law

Proof:

① $1.A = A$

1	2
A	1.A
0	0
1	1

From 1st & 2nd columns

$\boxed{1.A = A}$ //.

② $0 + A = A$

1	2
A	0+A
0	0
1	1

From 1st & 2nd columns

$\boxed{A = 0 + A}$

③ $0.A = 0$

1	2
A	0.A
0	0
1	0

From 2nd column output is zero always

$\therefore \boxed{0.A = 0}$

④ $1 + A = 1$

1	2
A	1+A
0	1
1	1

From 2nd column output is always 1.

$\therefore \boxed{1 + A = 1}$ //.

⑤ $A.A = A$

1	2
A	A.A
0	0
1	1

From 1st & 2nd columns

$\boxed{A.A = A}$ //.

⑥ $A + A = A$

1	2
A	A+A
0	0
1	1

From 1st & 2nd columns

$\boxed{A + A = A}$ //.

⑦ $A.\bar{A} = 0$

1	2	3
A	$\bar{A}$	$A\bar{A}$
0	1	0
1	0	0

From 3rd column output is always 0.

$\therefore \boxed{A\bar{A} = 0}$ //.

⑧ $A + \bar{A} = 1$

1	2	3
A	$\bar{A}$	$A+\bar{A}$
0	1	1
1	0	1

From 3rd column the output is always 1.

$\therefore \boxed{A + \bar{A} = 1}$ //.

⑨ $AB = BA$

1	2	3	4
A	B	AB	BA
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

From 3rd & 4th columns

$\boxed{AB = BA}$ //.

⑩ $A + B = B + A$

1	2	3	4
A	B	A+B	B+A
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	1

From 3rd & 4th columns

$\boxed{A + B = B + A}$

⑪ $(AB)C = A(BC)$

1	2	3	4	5	6	7
A	B	C	AB	BC	(AB)C	A(BC)
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	1	0	0	0
1	1	1	1	1	1	1

From 6th & 7th columns

$\boxed{(AB)C = A(BC)}$ //.

(12) $(A+B)+C = A+(B+C)$

1	2	3	4	5	6	7
A	B	C	A+B	B+C	(A+B)+C	A+(B+C)
0	0	0	0	0	0	0
0	0	1	0	1	1	1
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	1	0	1	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

From column 6th & 7th,

$\boxed{(A+B)+C = A+(B+C)}$ //.

(13) $A+BC = (A+B)(A+C)$

Method 1

$RHS = (A+B)(A+C)$

$= AA + AC + AB + BC$

$= A + AC + AB + BC$

$= A(1+C+B) + BC$

$= A + BC = LHS$

($\because AA = 1$, $1 + C + \cdots = 1$)

Method 2

1	2	3	4	5	6 X	7 Y	8
A	B	C	BC	A+BC	(A+B)	(A+C)	XY
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0
0	1	0	0	0	1	0	0
0	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1
1	0	1	0	1	1	1	1
1	1	0	0	1	1	1	1
1	1	1	1	1	1	1	1

From 5th & 8th column

$\boxed{A+BC = (A+B)(A+C)}$ //.

(14) $A(B+C) = AB+AC$

Method 1

$RHS = AB + AC$

$= A(B+C) = LHS$

Method 2

1	2	3	4	5	6	7	8
A	B	C	B+C (X)	AX	AB (Y)	AC (Z)	Y+Z
0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	1	1	1	0	1	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

From 5th & 8th column,

$\boxed{A(B+C) = AB+AC}$ //.

(15) $A(A+B) = A$

Method 1

$LHS = A(A+B)$

$= AA + AB$

$= A + AB$ ($\because AA = A$)

$= A(1+B)$

$= A$ ($\because 1+B = 1$)

$= RHS$

(15) Method 2

1	2	3	4
A	B	A+B	A(A+B)
0	0	0	0
0	1	1	0
1	0	1	1
1	1	1	1

From 1st & 4th Column,

$A(A+B) = A$ //.

(16) $A+AB = A$

Method 1

LHS = $A+AB$

$= A(1+B)$

$= A$ $\because 1+B=1$

$=$ RHS

Method 2

1	2	3	4
A	B	AB	A+AB
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	1

From 1st & 4th Column

$A+AB = A$ //.

Note:

(1) EX-OR = $\overline{\text{EX-NOR}}$

i.e $A \oplus B = \overline{A \odot B}$

(2) EX-NOR = $\overline{\text{EX-OR}}$

i.e $A \odot B = \overline{A \oplus B}$

(3) $\Rightarrow \bar{A}B + A\bar{B} = \overline{\bar{A}\bar{B} + AB}$

(4) $\bar{A}\bar{B} + AB = \overline{\bar{A}B + A\bar{B}}$

(5) $\bar{\bar{A}} = A$

Proof:

1	2	3
A	$\bar{A}$	$\bar{\bar{A}}$
0	1	0
1	0	1

From 1st & 3rd column.

$\bar{\bar{A}} = A$ //.

* De-Morgan's theorem (or) Laws

(1) $\overline{A.B} = \bar{A} + \bar{B}$

(or) The complement of a product is equal to the sum of the complements.

Proof:

1	2	3	4	5	6	7
A	B	$\bar{A}$	$\bar{B}$	$\bar{A}+\bar{B}$	AB	$\overline{AB}$
0	0	1	1	1	0	1
0	1	1	0	1	0	1
1	0	0	1	1	0	1
1	1	0	0	0	1	0

From 5th & 7th columns, $\overline{A.B} = \bar{A} + \bar{B}$ //.

② $\overline{A+B} = \bar{A} \cdot \bar{B}$ (or)

The complement of a sum is equal to the product of the complements.

Proof:

1	2	3	4	5	6	7
A	B	$\bar{A}$	$\bar{B}$	$\bar{A}\cdot\bar{B}$	A+B	$\overline{A+B}$
0	0	1	1	1	0	1
0	1	1	0	0	1	0
1	0	0	1	0	1	0
1	1	0	0	0	1	0

From 5th & 7th columns $\overline{A+B} = \bar{A} \cdot \bar{B}$

Note:

① DeMorgan's theorems for 3 variables

(a) $\overline{ABC} = \bar{A}+\bar{B}+\bar{C}$ (b) $\overline{A+B+C} = \bar{A}\cdot\bar{B}\cdot\bar{C}$

② DeMorgan's theorems for 4 variables

(a) $\overline{ABCD} = \bar{A}+\bar{B}+\bar{C}+\bar{D}$ (b) $\overline{A+B+C+D} = \bar{A}\cdot\bar{B}\,\bar{C}\,\bar{D}$

③ DeMorgan's theorems for N variables

(a) $\overline{ABCD\ldots N} = \bar{A}+\bar{B}+\bar{C}+\ldots+\bar{N}$

(b) $\overline{A+B+C+\ldots+N} = \bar{A}\cdot\bar{B}\cdot\bar{C}\ldots\bar{N}$

Proof: ①

$2^N = 2^3 = 8$ combinations

*2 variable = N

$2^N = 2^2 = 4$ combinations

②

$2^4 = 16$ combinations

③ AND, OR, NOT gates → Basic gates

④ NAND, NOR → Universal gates (Any logic gate can be realized)

Proof of ① (a)

1 A	2 B	3 C	4 ABC	5 $\overline{ABC}$	6 $\bar{A}$	7 $\bar{B}$	8 $\bar{C}$	9 $\bar{A}+\bar{B}+\bar{C}$
0	0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0	1
0	1	0	0	1	1	0	1	1
0	1	1	0	1	1	0	0	1
1	0	0	0	1	0	1	1	1
1	0	1	0	1	0	1	0	1
1	1	0	0	1	0	0	1	1
1	1	1	1	0	0	0	0	0

From 5th & 9th column $\overline{ABC} = \bar{A}+\bar{B}+\bar{C}$ //

(b)

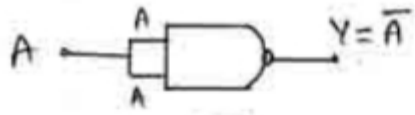
1 A	2 B	3 C	4 $\bar{A}$	5 $\bar{B}$	6 $\bar{C}$	7 $\bar{A}.\bar{B}.\bar{C}$	8 A+B+C	9 $\overline{A+B+C}$
0	0	0	1	1	1	1	0	1
0	0	1	1	1	0	0	1	0
0	1	0	1	0	1	0	1	0
0	1	1	1	0	0	0	1	0
1	0	0	0	1	1	0	1	0
1	0	1	0	1	0	0	1	0
1	1	0	0	0	1	0	1	0
1	1	1	0	0	0	0	1	0

From 7th & 9th Column. $\overline{A+B+C} = \bar{A}.\bar{B}.\bar{C}$ //

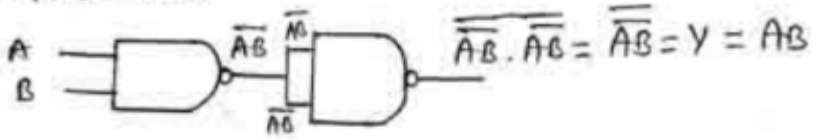
Problems:

1) Realise the following gates using NAND gates
(a) NOT gate (b) AND gate (c) OR gate (d) NOR gate
(e) EX-OR gate (f) EX-NOR gate

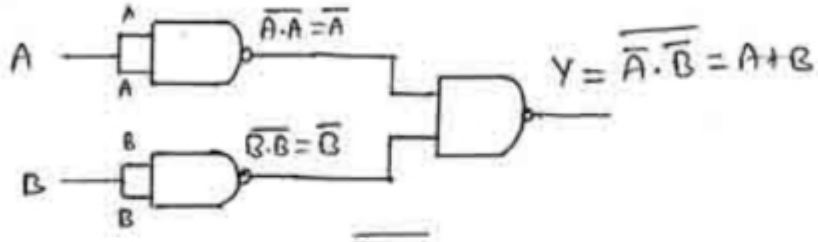
Sol: (a) $Y = \bar{A} = \overline{A.A}$ $(\because A.A = A)$



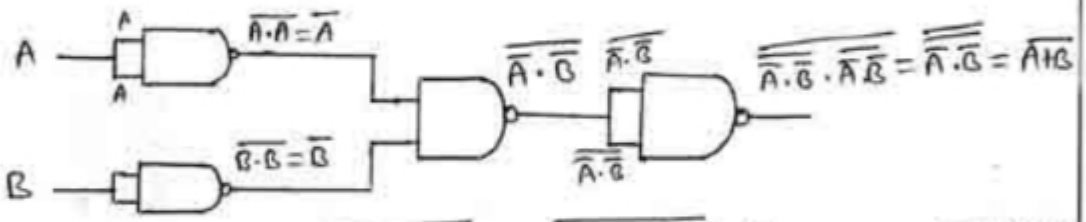
(b) $Y = AB = \overline{\overline{AB}}$



(c) $Y = A+B = \overline{\overline{A+B}} = \overline{\overline{A} \cdot \overline{B}}$

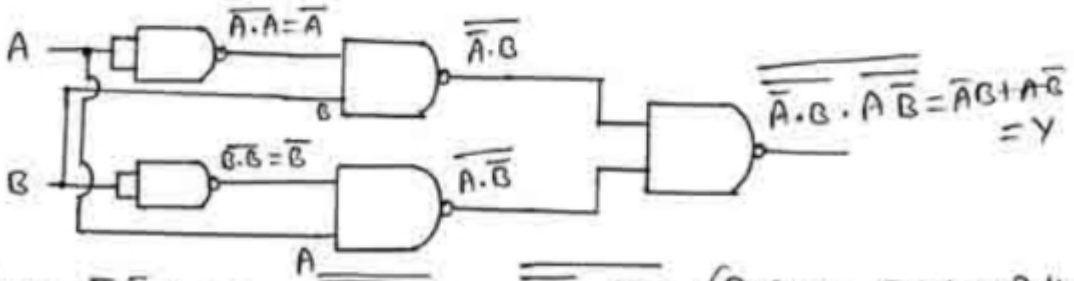


(d) $Y = \overline{A+B} = \overline{A} \cdot \overline{B} = \overline{\overline{\overline{A} \cdot \overline{B}}}$



(e) $Y = \overline{A}B + A\overline{B} = \overline{\overline{\overline{A}B + A\overline{B}}} = \overline{\overline{A}B} \cdot \overline{A\overline{B}}$ (Requires 5 NAND gates)

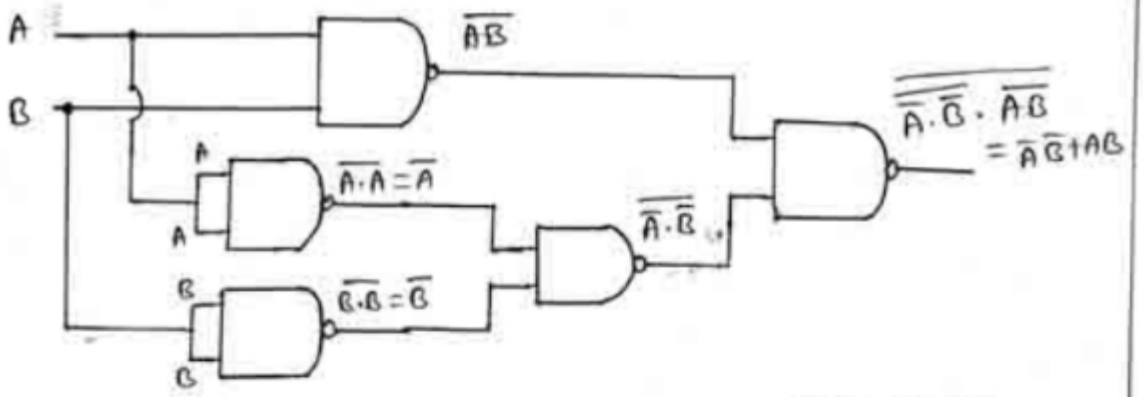
(f) $Y = \overline{\overline{A}\overline{B} + AB} = \overline{\overline{A}B} \cdot \overline{AB}$ (Requires 6 NAND gates)



(g) $Y = \overline{A}\overline{B} + AB = \overline{\overline{A}\overline{B} + AB} = \overline{\overline{A}\overline{B}} \cdot \overline{AB}$ (Requires 5 NAND gates)

(h) $Y = \overline{A}B + A\overline{B} = \overline{A}B \cdot \overline{AB} = \overline{\overline{A}B} \cdot \overline{A\overline{B}}$ (Requires 6 NAND gates)

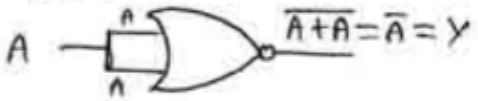
Note: EX-OR gate = EX-NOR gate & Vice Versa



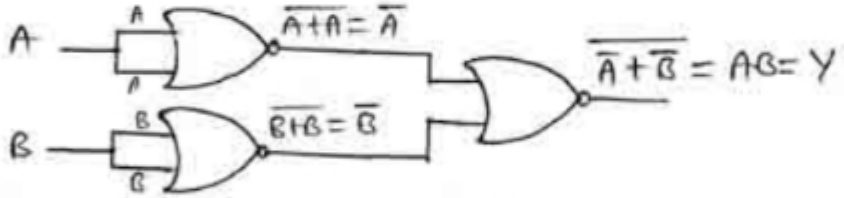
② Realise the following gates using NOR gates
ⓐ NOT ⓑ AND ⓒ OR ⓓ NAND ⓔ EX-OR ⓕ EX-NOR

Sol:

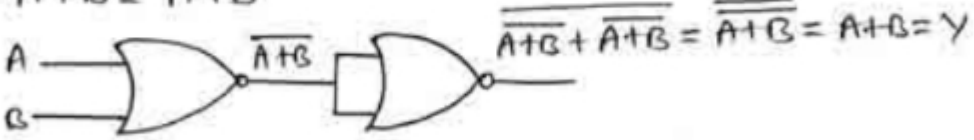
ⓐ $Y=\overline{A}=\overline{A+A}$ $(\because A+A=A)$



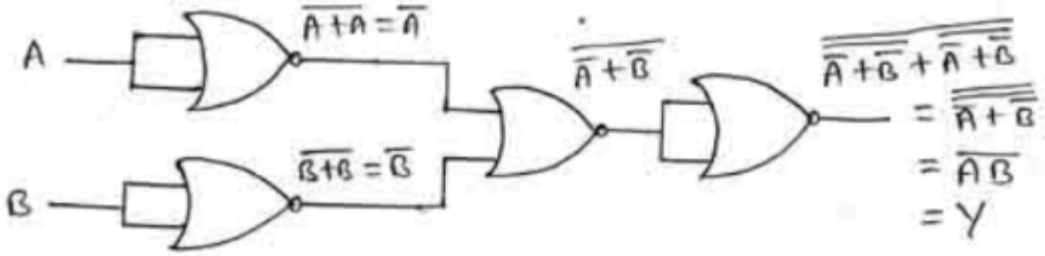
ⓑ $Y=AB=\overline{\overline{A}\,\overline{B}}=\overline{\overline{A}+\overline{B}}$



ⓒ $Y=A+B=\overline{\overline{A+B}}$



ⓓ $Y=\overline{AB}=\overline{A}+\overline{B}=\overline{\overline{\overline{A}+\overline{B}}}$

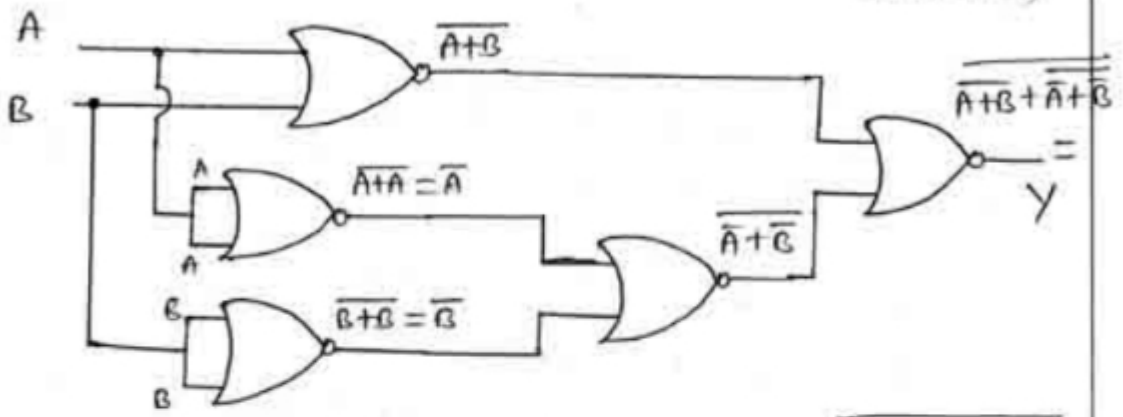


(e) $Y = \bar{A}B + A\bar{B} = \overline{\bar{A}B} + \overline{A\bar{B}} = \overline{\bar{A}+\bar{B}} + \overline{A+\bar{B}}$

(or) $= \overline{\overline{A+\bar{B}} + \overline{\bar{A}+B}}$ (6 Gates required)

$Y = \overline{\bar{A}\bar{B} + AB} = \overline{\bar{A}\bar{B}} + \overline{AB} = \overline{\bar{A}+\bar{B}} + \overline{\bar{A}+\bar{B}}$

$= \overline{\overline{A+B} + \overline{\bar{A}+\bar{B}}}$ (5 Gates required)

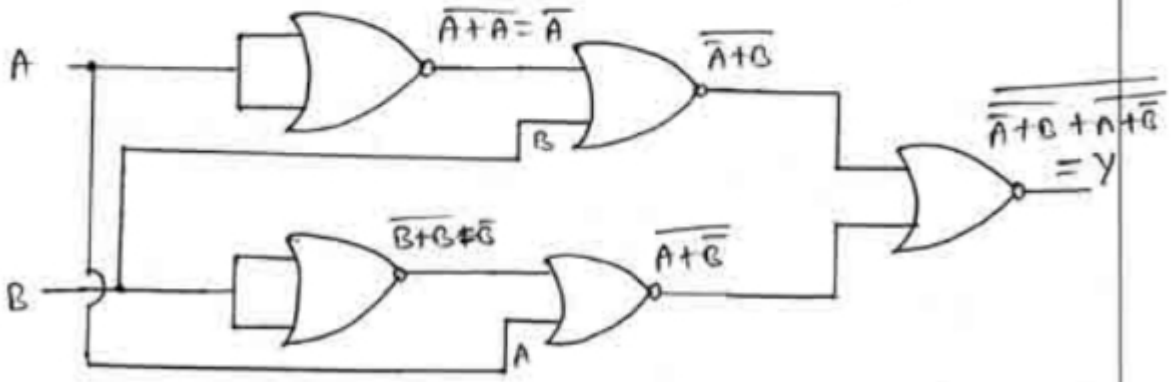


(f) $Y = \bar{A}\bar{B} + AB = \overline{\bar{A}\bar{B}} + \overline{AB} = \overline{\bar{A}+\bar{B}} + \overline{\bar{A}+B} = \overline{\overline{A+B} + \overline{\bar{A}+\bar{B}}}$

(6 Gates required)

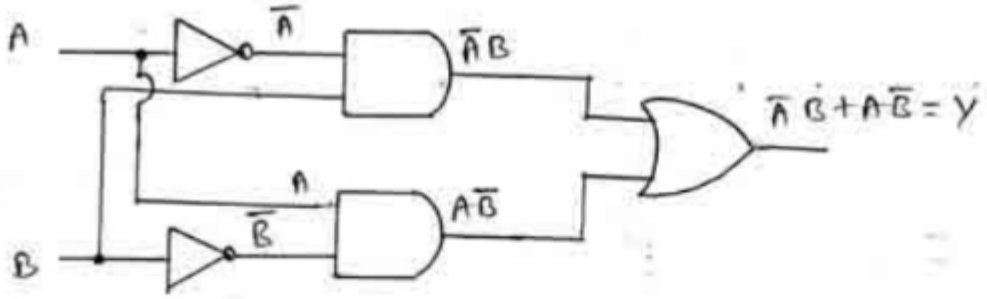
(or) $Y = \overline{\bar{A}B + A\bar{B}} = \overline{\bar{A}B} + \overline{A\bar{B}} = \overline{\bar{A}+\bar{B}} + \overline{\bar{A}+B} = \overline{\overline{A+\bar{B}} + \overline{\bar{A}+B}}$

(5 gates required)



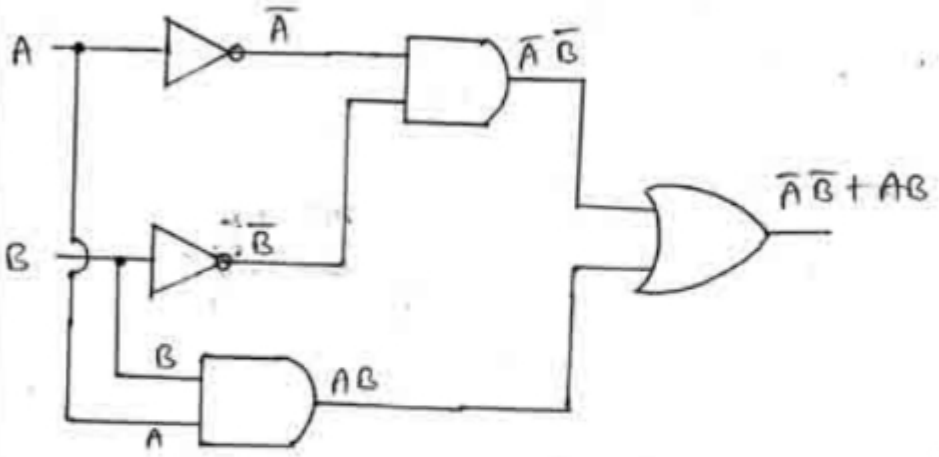
(3) Realize EX-OR & EX-NOR gates using basic gates.

Ans: EX-OR. $Y = \bar{A}B + A\bar{B}$ (or) $\overline{\bar{A}\bar{B} + AB}$



EX-NOR

$Y = \bar{A}\bar{B} + AB$ or $\overline{\bar{A}B + A\bar{B}}$



(4) Construct the truth table for the following Boolean expressions.

(a) $Y = \overline{AB + \bar{A} + \bar{A}B}$ (b) $Y = \overline{\overline{\bar{A}B + AB}}$ (c) $Y = A(\bar{B}+\bar{C})$

Sol: (a)

A	B	$\bar{A}$ (X)	AB (Z)	$\bar{A}B$ (P)	X+Z+P	$Y=\overline{X+Z+P}$
0	0	1	0	1	1	0
0	1	1	0	1	1	0
1	0	0	0	1	1	0
1	1	0	1	0	1	0

(b) $Y = \overline{\overline{\bar{A}B + AB}} = \bar{A}B + AB$

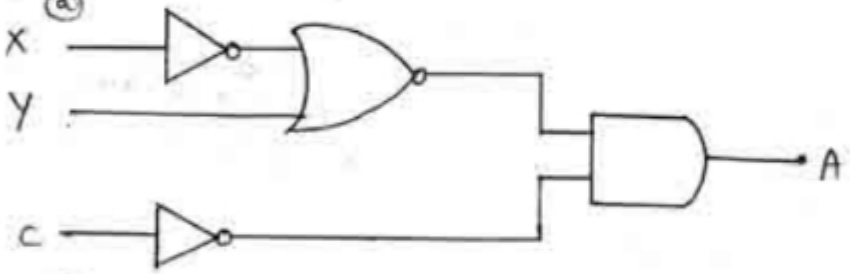
A	B	AB	$\bar{A}B$	$Y=\bar{A}B+AB$
0	0	0	1	1
0	1	0	1	1
1	0	0	1	1
1	1	1	0	1

(c) $Y = A(\bar{B} + \bar{C})$

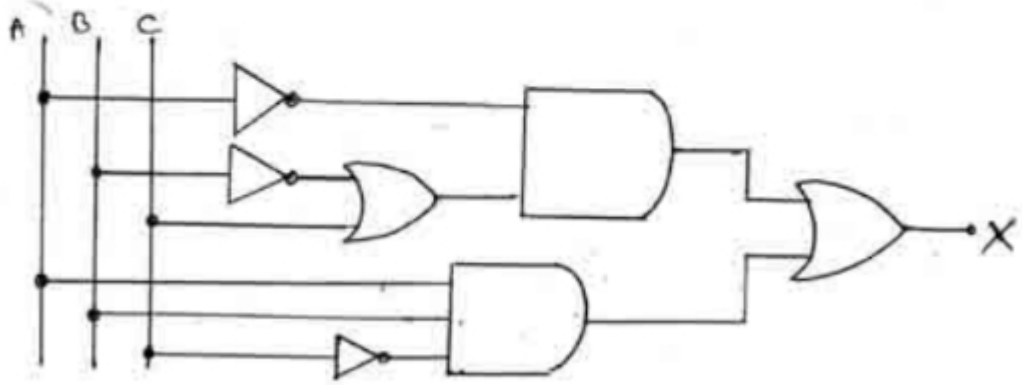
A	B	C	$\bar{B}$	$\bar{C}$	$\bar{B}+\bar{C}$	$A(\bar{B}+\bar{C})$
0	0	0	1	1	1	0
0	0	1	1	0	1	0
0	1	0	0	1	1	0
0	1	1	0	0	0	0
1	0	0	1	1	1	1
1	0	1	1	0	1	1
1	1	0	0	1	1	1
1	1	1	0	0	0	0

5) Write the Boolean expressions for the logic diagram shown below.

(a)



(b)

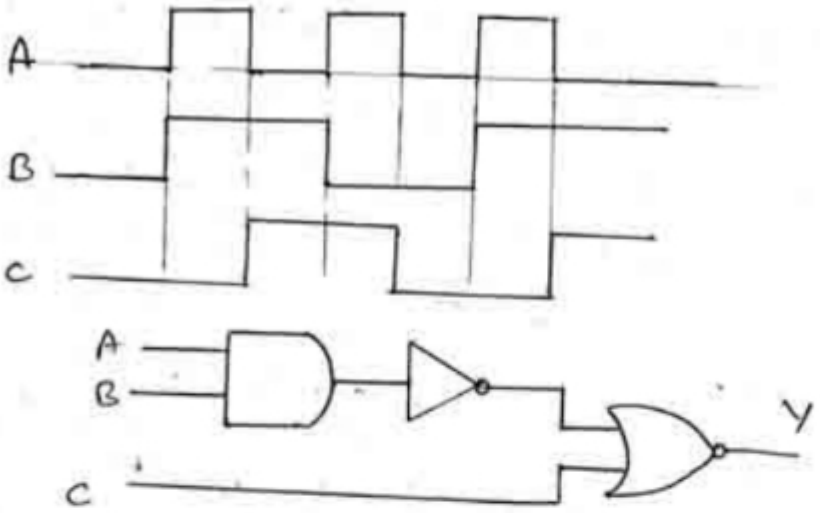


Sol:

(a) $A = (\overline{\bar{X} + Y})\,\bar{C}$

(b) $X = [\bar{A}\,(\bar{B}+C)] + A\,B\,\bar{C}$

6) Draw the output waveform of the logic circuit shown for the following input waveforms.



Sol:

From the given Logic circuit,

$$Y = \overline{\overline{AB} + C}$$

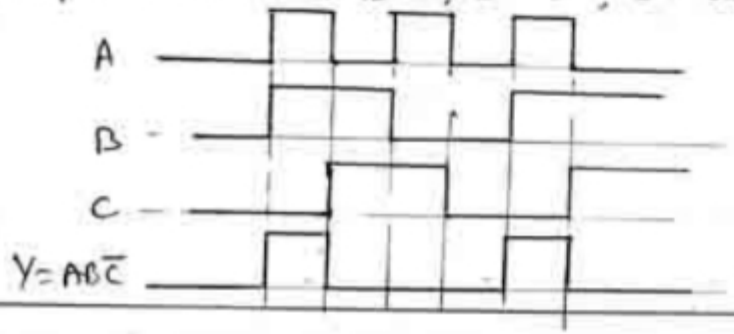
$$\Rightarrow Y = \overline{\bar{A} + \bar{B} + C}$$

$$= \bar{\bar{A}} \cdot \bar{\bar{B}} \cdot \bar{C}$$

$$= AB\bar{C}$$

A	B	C	AB	$\bar{C}$	$Y = AB\bar{C}$
0	0	0	0	1	0
0	0	1	0	0	0
0	1	0	0	1	0
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	0	0	0
1	1	0	1	1	1
1	1	1	1	0	0

From truth table it is clear that output $Y = 1$ only when $A = 1, B = 1, C = 0$, otherwise output $(Y) = 0$



7) Prove the following Boolean expressions

(a) $A+\bar{A}B = A+B$ (b) $\bar{A}+AB = \bar{A}+B$

(c) $A+\bar{A}B+AB\bar{C} = A+B$ (d) $A+\bar{A}B+ABC+A\bar{C} = A+B$

(e) $\overline{AB+\bar{A}\bar{B}}+A = 0$ (f) $AB+\bar{A}+\bar{A}\bar{B} = 1$

(g) $ABC+A\bar{B}C+AB\bar{C} = AB+AC$ (h) $\bar{A}\bar{B}+\bar{A}+AB = 0$

(i) $AB+A+A\bar{B} = A$ (j) $\bar{x}\bar{y}\bar{z}+\bar{x}\bar{y}z+\bar{x}\bar{y}+x\bar{y} = \bar{y}$

Sol: Method I

(a) LHS $= A+\bar{A}B$

$= A\cdot 1+\bar{A}B$

$= A.(1+B)+\bar{A}B \quad (\because 1+B=1)$

$= A+AB+\bar{A}B$

$= A+B(A+\bar{A}) \quad (\because A+\bar{A}=1)$

$= A+B\cdot 1$

$= A+B = RHS$

Method II (Method of Perfect Induction)

(a)

1	2	3	4	5	6
A	B	$\bar{A}$	$\bar{A}B$	$A+\bar{A}B$	$A+B$
0	0	1	0	0	0
0	1	1	1	1	1
1	0	0	0	1	1
1	1	0	0	1	1

From 5th & 6th Column.

$A+\bar{A}B = A+B$ //

(b) LHS $= \bar{A}+AB = \bar{A}(1+B)+AB = \bar{A}+\bar{A}B+AB = \bar{A}+B(A+\bar{A})$

$= \bar{A}+B$

$= RHS$

(c) LHS $= A+\bar{A}B+AB\bar{C}$

$= A(1+B\bar{C})+\bar{A}B$

$= A+\bar{A}B \quad [\because 1+B\bar{C}=1]$

$= A(1+B)+\bar{A}B \quad [1+B=1]$

$= A+AB+\bar{A}B \quad [A+\bar{A}=1]$

$= A+B(A+\bar{A}) = A+B = RHS$

(d) LHS = $A + \bar{A}B + ABC + A\bar{C}$

$= A(1 + BC + \bar{C}) + \bar{A}B$ $(\because 1 + \text{Anything} = 1)$

$= A + \bar{A}B$

$= A + B$ $(\because A + \bar{A}B = A + B)$

$=$ RHS

(e) LHS = $\overline{\bar{A}B + \bar{A}\bar{B} + A}$

$= \bar{A}\bar{B} \cdot \overline{\bar{A}\bar{B}} \cdot \bar{A}$ [Demorgan's theorem $\overline{A+B+C} = \bar{A}\bar{B}\bar{C}$]

$= \bar{A}\bar{B} \cdot AB \cdot \bar{A}$

$= 0$ $[\because A\bar{A} = 0$ and $AB \cdot \bar{A}\bar{B} = 0]$

$=$ RHS

(f) LHS = $AB + A + \bar{A}\bar{B}$

$= AB + \bar{A}\bar{B} + \bar{A}$

$= 1 + \bar{A}$ $[\because A + \bar{A} = 1$ and $AB + \bar{A}\bar{B} = 1]$

$= 1$ $[1 + \text{Anything} = 1]$

$=$ RHS

(g) LHS = $ABC + A\bar{B}C + AB\bar{C}$

$= AC(B + \bar{B}) + AB\bar{C}$

$= AC + AB\bar{C}$ $(\because B + \bar{B} = 1)$

$= A(C + \bar{C}B)$

$= A(C + B)$ $(\because C + \bar{C}B = C + B)$

$= AB + AC$

$=$ RHS

(h) LHS = $\overline{\bar{A}B + \bar{A} + AB} = \bar{\bar{A}}B \cdot \bar{\bar{A}} \cdot \overline{AB} = AB \cdot A\overline{AB} = 0 = RHS$

($\because AB \cdot \overline{AB} = 0$)

(i) LHS = $AB + A + AB = A(B + 1 + B) = A = RHS$

[$\because 1 + Anything = 1$]

(j)

LHS = $\bar{X}\bar{Y}\bar{Z} + \bar{X}\bar{Y}Z + \bar{X}\bar{Y} + X\bar{Y}$

$= \bar{X}\bar{Y}\bar{Z} + \bar{X}\bar{Y} + X\bar{Y}$ ($\because A + A = A$ IIIrd $\bar{X}\bar{Y}\bar{Z} + \bar{X}\bar{Y}Z = \bar{X}\bar{Y}$)

$= \bar{X}\bar{Y}(\bar{Z} + 1) + X\bar{Y}$

$= \bar{X}\bar{Y} + X\bar{Y}$ ($\because \bar{Z} + 1 = 1$)

$= \bar{Y}(\bar{X} + X)$ ($\because X + \bar{X} = 1$)

$= \bar{Y}$

$= RHS$

8) Simplify (factorize) the following Boolean expressions

(a) $\bar{A}C + \overline{AC}$ (b) $AB + \bar{A}C + \bar{B}C$ (c) $(A + \bar{B}C)(A\bar{B} + C)$

(d) $(\overline{A+B})(\bar{A} + \bar{C})(\bar{B} + C)$ (e) $AB + ABC + \bar{A}B + A\bar{B}C$

Sol

(a) Let $Y = \bar{A}C + \overline{AC} = \bar{A}C + \bar{A} + \bar{C} = \bar{A}(C + 1) + \bar{C}$

$= \bar{A} + \bar{C} \oplus \overline{AC}$

(b) Let $Y = AB + \bar{A}C + \bar{B}C$

$= AB + C(\bar{A} + \bar{B})$

$= AB + C\overline{AB}$

$= AB + C$ [$\because A + \bar{A}C = A + C$ IIIrd $AB + \overline{AB}C = AB + C$]

(c) $(A+\bar{B}C)(A\bar{B}+C)$

$= A A\bar{B} + AC + A\bar{B}\bar{B}C + \bar{B}CC$

$= A\bar{B} + AC + A\bar{B}C + \bar{B}C$ $\left[\because AA = A,\ \bar{B}\bar{B} = \bar{B},\ CC = C\right]$

$= A\bar{B} + AC + \bar{B}C(A+1)$

$= A\bar{B} + \bar{B}C + CA$ $(\because A+1 = 1)$

(d) $\overline{(A+B)}(\bar{A}+\bar{C})(\bar{B}+C)$

$= (\bar{A}\cdot\bar{B})(\bar{A}\bar{B} + \bar{A}C + \bar{B}\bar{C} + C\bar{C})$

$= \bar{A}\bar{B}\bar{A}\bar{B} + \bar{A}\bar{A}\bar{B}C + \bar{A}\bar{B}\bar{B}\bar{C}$

$= \bar{A}\bar{B} + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}$

$= \bar{A}\bar{B}(1 + C + \bar{C})$

$= \bar{A}\bar{B}$

(e) $AB + ABC + \bar{A}B + A\bar{B}C$

$= AB(1+C) + \bar{A}B + A\bar{B}C$

$= AB + \bar{A}B + A\bar{B}C$

$= B(A+\bar{A}) + A\bar{B}C$

$= B + A\bar{B}C$

$= B + AC$

3) Simplify the following Boolean equations & draw the logic diagram

(a) $Y = A\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C}$ (b) $\bar{X}\bar{Y}\bar{Z} + \bar{X}Y\bar{Z} + \bar{Y}\bar{Z} + X\bar{Z}$

(c) $ABC + A\bar{B}C + AB\bar{C} + \bar{A}BC$

Sol

(a) Given $Y = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C}$

$= \overline{A+B+C} + \overline{(A+B+A)C}$

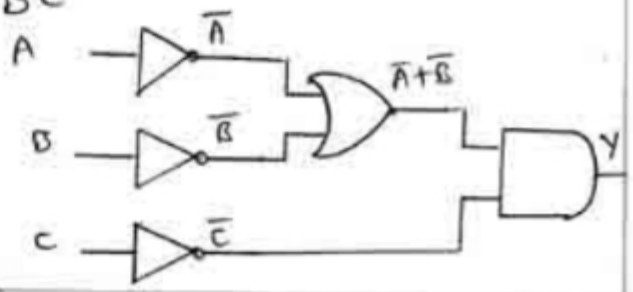
$= \bar{A}\bar{C}(\bar{B}+B) + A\bar{B}\bar{C}$

$= \bar{A}\bar{C} + A\bar{B}\bar{C}$

$= \bar{C}(\bar{A} + A\bar{B})$

$= \bar{C}(\bar{A} + \bar{B})$

$= \bar{C}\bar{A} + \bar{C}\bar{B}$ (or) //..



(b) Let $A = \bar{x}\bar{y}\bar{z} + \overline{xy}\,\bar{z} + \bar{y}\bar{z} + x\bar{z}$

$= \bar{y}\bar{z}(\bar{x}+1) + (\bar{x}+\bar{y})\bar{z} + x\bar{z}$

$= \bar{y}\bar{z} + \bar{x}\bar{z} + \bar{y}\bar{z} + x\bar{z}$

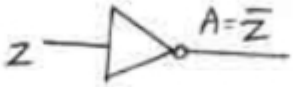
$= \bar{y}\bar{z} + \bar{x}\bar{z} + x\bar{z}$

$= \bar{y}\bar{z} + \bar{z}(\bar{x}+x)$

$= \bar{y}\bar{z} + \bar{z}$

$= \bar{z}(\bar{y}+1)$

$= \bar{z}$ //



(c) Let $X = ABC + A\bar{B}C + AB\bar{C} + \bar{A}BC$

$= AC(B+\bar{B}) + AB\bar{C} + \bar{A}BC$

$= AC + AB\bar{C} + \bar{A}BC$

$= A(C + B\bar{C}) + \bar{A}BC$

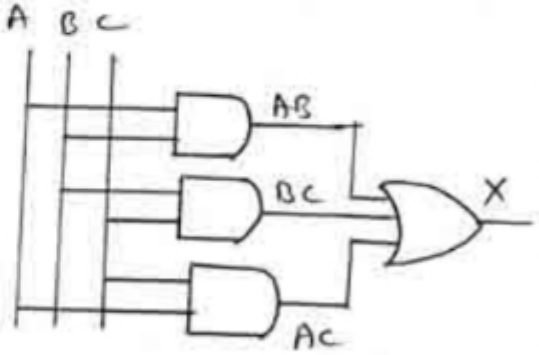
$= A(C+B) + \bar{A}BC$

$= AC + AB + \bar{A}BC$

$= AC + B(A + \bar{A}C)$

$= AC + B(A+C)$

$= AC + BA + BC$



(iv) Simplify & realize using only NAND gate the following Boolean expressions.

(a) $Y = (A+B+C)(A+B)$ (b) $Y = AB + ABC + AB\bar{C}$

(c) $(A+\bar{B}C)(\bar{A}+B+\bar{C})(A+\bar{B})$

Sol (a) $Y = (A+B+C)(A+B)$

$= AA + AB + BA + BB + CA + CB$

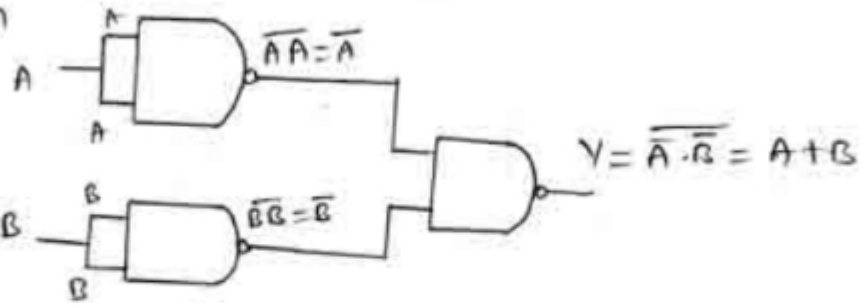
$= A + AB + B + CA + CB$

$= A(1 + B + C) + B(1 + C)$

$\boxed{Y = A + B}$

Now $Y = A + B = \overline{\overline{A + B}} = \overline{\bar{A} \cdot \bar{B}}$

Realization



(b) Given $Y = AB + ABC + AB\bar{C}$

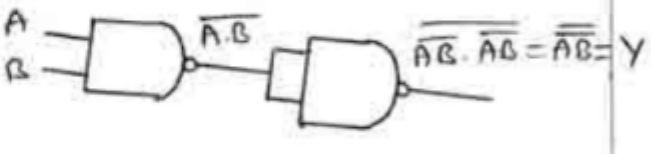
$= AB(1 + C + \bar{C})$

$\boxed{Y = AB}$ //

Realization

Now

$Y = AB = \overline{\overline{AB}}$



(c) Let $X = (A + \bar{B}C)(\bar{A} + B + \bar{C})(A + \bar{B})$

$= (A\bar{A} + AB + A\bar{C} + \bar{A}\bar{B}C + B\bar{B}C + \bar{B}C\bar{C})(A + \bar{B})$

$= (AB + A\bar{C} + \bar{A}\bar{B}C)(A + \bar{B})$

$= AAB + AB\bar{B} + AA\bar{C} + A\bar{B}\bar{C} + A\bar{A}\bar{B}C + \bar{A}\bar{B}\bar{B}C$

$= AB + A\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}C$

$= AB + A\bar{C}(1 + \bar{B}) + \bar{A}\bar{B}C$

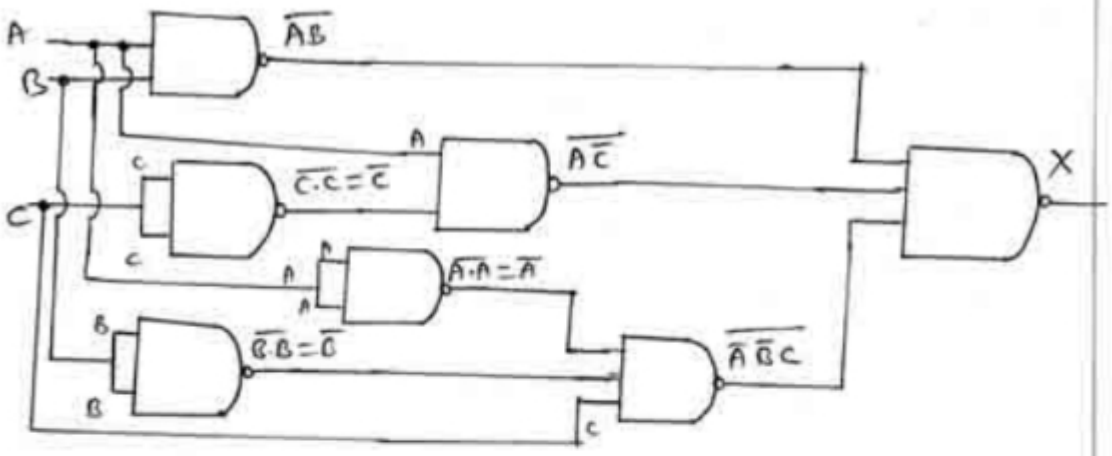
$\boxed{X = AB + A\bar{C} + \bar{A}\bar{B}C}$ //

Now

$X = AB + A\bar{C} + \bar{A}\bar{B}C = \overline{\overline{AB + A\bar{C} + \bar{A}\bar{B}C}}$

$$X = \overline{\overline{A}B} \cdot \overline{A\overline{C}} \cdot \overline{\overline{A}\,\overline{B}C}$$

Realization



(11) Simplify & implement the following expressions using only NOR gates

(a) $Y = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}\,D + A\,\overline{B}\,\overline{C}\,\overline{D} + A\,\overline{B}\,\overline{C}\,D$

(b) $Y = \overline{(A+\overline{B}+C)(\overline{A}+B+C)(A+B)}$

(c) $X = \overline{A}BC + A\,\overline{B}\,C + A\,BC$

Sol

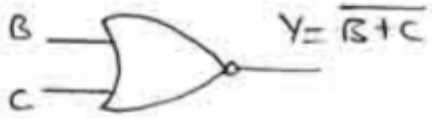
(a) $Y = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}\,D + A\,\overline{B}\,\overline{C}\,\overline{D} + A\,\overline{B}\,\overline{C}\,D$

$= \overline{B}\,\overline{C}(\overline{A}\,\overline{D} + \overline{A}\,D + A\,\overline{D} + AD)$

$= \overline{B}\,\overline{C}\,[\overline{A}(\overline{D}+D)' + A(\overline{D}+D)']$

$= \overline{B}\,\overline{C}\,(\overline{A}+A)'$

$\boxed{Y = \overline{B}\,\overline{C}}$ //



Now $Y = \overline{B}\,\overline{C} = \overline{B+C}$

(b) $Y = \overline{(A+\bar{B}+C)(\bar{A}+B+C)(A+B)}$

$= \overline{(A\bar{A} + AB + Ac + \bar{A}\bar{B} + B\bar{B} + \bar{B}C + \bar{A}C + BC + CC)(A+B)}$

$= \overline{(AB + Ac + \bar{A}\bar{B} + \bar{B}C + \bar{A}C + BC + C)(A+B)}$

$= \overline{(AB + \bar{A}\bar{B} + C(A + \bar{B} + \bar{A} + B + 1))(A+B)}$

$= \overline{(AB + \bar{A}\bar{B} + C)(A+B)}$

$= \overline{AAB + ABB + A\bar{A}\bar{B} + \bar{A}B\bar{B} + CA + CB}$

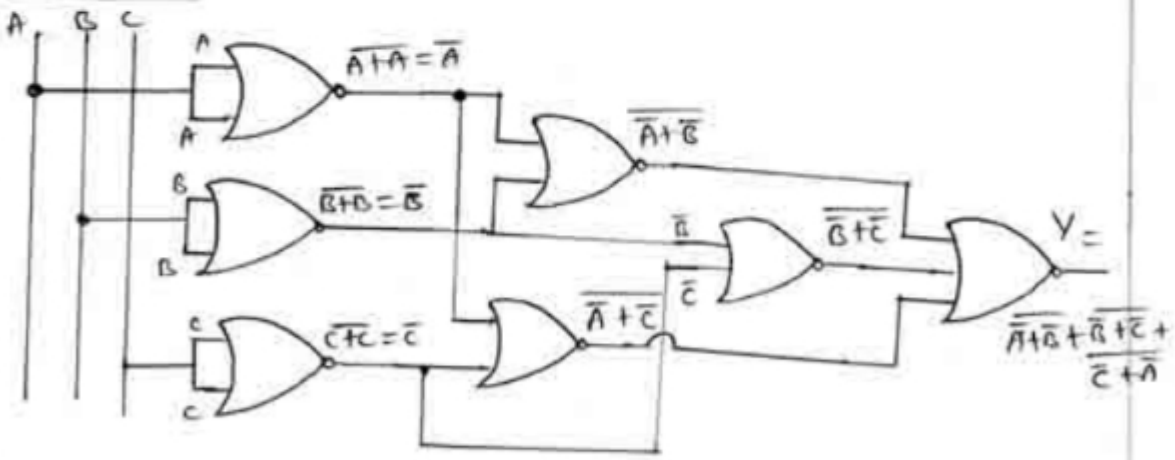
$= \overline{AB + AB + CA + CB}$

$\boxed{Y = \overline{AB + BC + CA}}$

Now $Y = \overline{\overline{AB} + \overline{BC} + \overline{CA}}$

$= \overline{\overline{A} + \overline{B} + \overline{B} + \overline{C} + \overline{C} + \overline{A}}$

Realization



(c) $Y = \bar{A}BC + A\bar{B}C + ABC$

$= \bar{A}BC + Ac(\bar{B} + B)$

$= \bar{A}BC + Ac$

$= c(\bar{A}B + A) = c(A+B) \Rightarrow CA + CB$ //

NOR $Y = \overline{C(A+B)}$

$= \overline{\overline{C} + \overline{A+B}}$

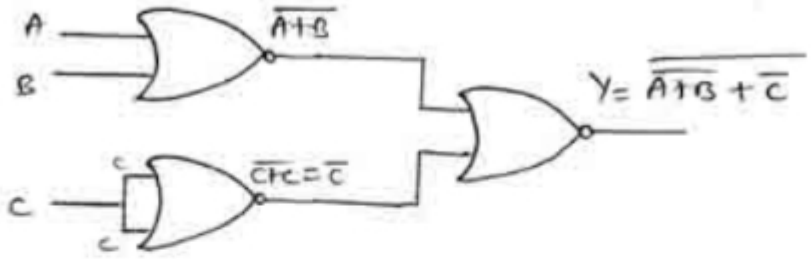
(3 NOR gates required)

(a) $Y = \overline{CA} + \overline{CB}$

$= \overline{\overline{C}+\overline{A}} + \overline{\overline{C}+\overline{B}}$

(7 NOR gates required)

Realization



Half adder:

Definition: A Logic circuit which adds two binary variables (two bits), yields a carry but does not accept carry from another circuit (adder) is called a half adder

Block diagram

Fig①

Boolean expressions for Sum & Carry

Sum is 1 when A=1, B=0

& when A=0, B=1

$\therefore S = \overline{A}B + A\overline{B}$

(a) $S = A \oplus B$

Truth table

The truth table of a half-adder with inputs A and B and outputs Sum 'S' & Carry 'C' is shown in fig②

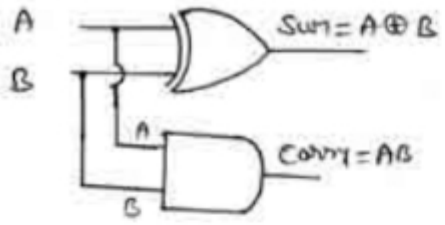
inputs		outputs	
A	B	Sum S	Carry C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Fig②

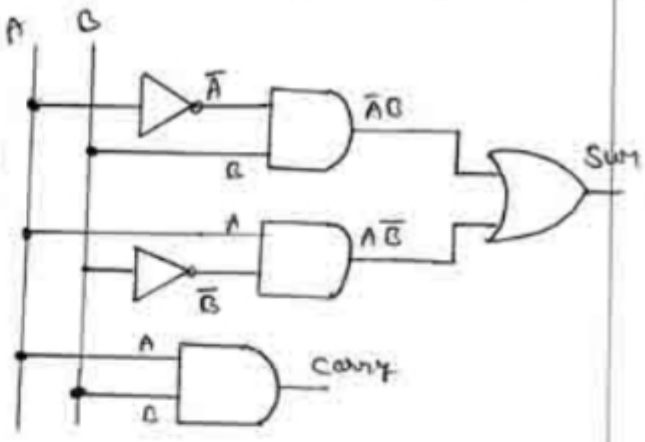
Carry is 1 when A = B = 1

$\therefore C = AB$

Implementation:



(or)



Limitation:

Addition of three bits cannot be done.

* Full adder:

Definition: A Logic circuit which adds two binary numbers (two bits), accept a carry and yield a carry is called **Full adder**

Block diagram

Fig ①

Boolean expressions for Sum(S) & Carry(Cout)

Sum is 1 when A=0, B=0, C_{in}=1, A=0, B=1, C_{in}=0, A=1, B=0, C_{in}=0 & A=B=C_{in}=1

Truth table

The truth table of a full adder with inputs A, B, & C_{in} and outputs Sum 'S' & Carry 'Cout' is shown in fig ②

← Inputs → ← Outputs →

A	B	C_{in}	Sum S	Carry Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$\therefore S = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$

$= (\bar{A}\bar{B} + AB)C_{in} + (\bar{A}B + A\bar{B})\bar{C}_{in}$ — ①

Let $X = \bar{A}B + A\bar{B}$ — ② $\Rightarrow \bar{X} = \bar{A}\bar{B} + AB$ — ③ $[X = A \oplus B]$

Using ② & ③ in ①, we get

$S = \bar{X}C_{in} + X\bar{C}_{in}$

$S = X \oplus C_{in}$

$\Rightarrow \boxed{S = A \oplus B \oplus C_{in}}$ // — ①

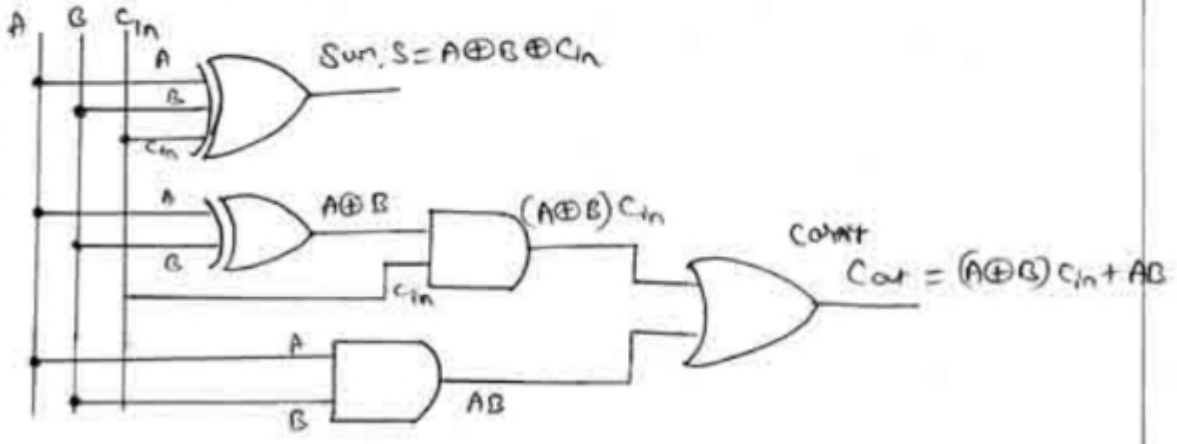
Carry is 1 when $A=0, B=1, C_{in}=1$, $A=1, B=0, C_{in}=1$, $A=1, B=1, C_{in}=0$ & $A=B=C_{in}=1$

$\therefore C_{out} = \bar{A}BC_{in} + A\bar{B}C_{in} + AB\bar{C}_{in} + ABC_{in}$

$C_{out} = (A\bar{B} + \bar{A}B)C_{in} + AB(\bar{C}_{in} + C_{in})$

$\boxed{C_{out} = (A \oplus B)C_{in} + AB}$ — ②

Implementation:



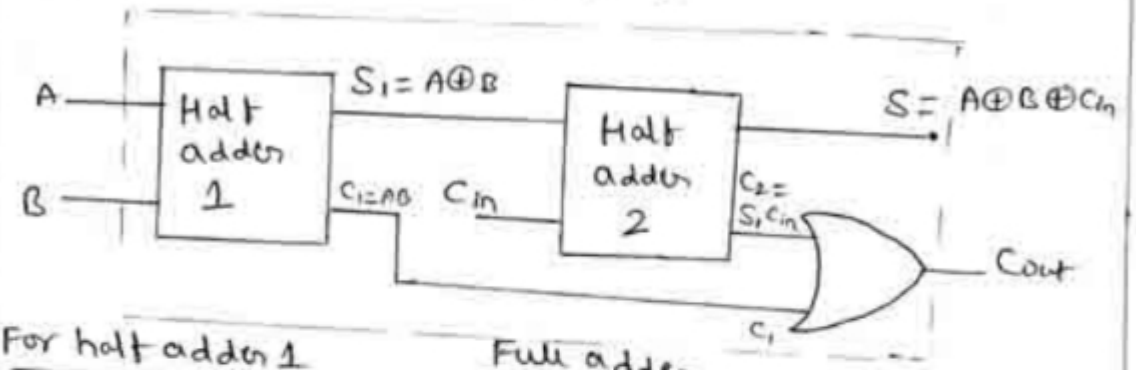
Advantage:

Addition of three bits can be done

* Implementation of Full adder using half-adders

(or) Implementation of Full adder using half-adders & NOR gate

Implementation of Full adder using half adders is shown below (BLOCK diagram)



Full adder

For half adder 1

Sum, $S_1 = A \oplus B$ — ③

Carry, $C_1 = AB$ — ④

For half adder 2:

(From ③ & ④)

Sum, $S = S_1 \oplus C_{in} = A \oplus B \oplus C_{in}$ — ⑤ [Same as ①]

Carry, $C_2 = S_1 C_{in} = (A \oplus B) C_{in}$ — ⑥

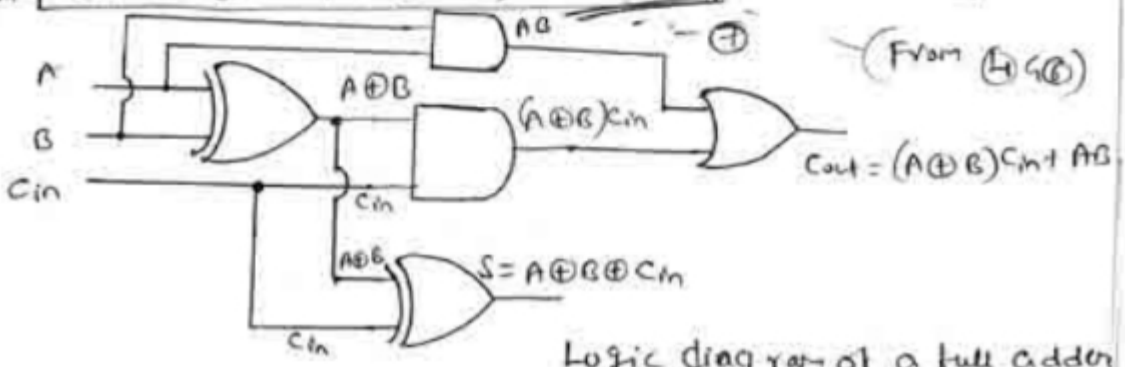
(From ③ & ⑤)

DR gate output

Carry out: $C_{out} = C_2 + C_1 = (A \oplus B) C_{in} + AB$ [Same as ②]

AB — ⑦

(From ④ & ⑥)



Logic diagram of a full adder

* Properties of logic gates & Characteristics

① Noise Margin ② Fan-in ③ Fan-out

④ Propagation delay ⑤ Power dissipation.

① For each element x in a Boolean algebra

ⓐ $x+1=1$ ⓑ $x.0=0$

Sol: ⓐ

$$\begin{aligned} LHS &= x+1 \\ &= 1.(x+1) \\ &= (x+\bar{x})(x+1) \\ &= x+(\bar{x}.1) \\ &= x+\bar{x} \\ &= 1 \\ &= RHS \end{aligned}$$

ⓑ

$$\begin{aligned} LHS &= x.0 \\ &= 0+(x.0) \\ &= (x.\bar{x})+(x.0) \\ &= x.(\bar{x}+0) \\ &= x.\bar{x} \\ &= 0 \\ &= RHS \end{aligned}$$

② For each element x in a Boolean algebra

ⓐ $x+x=x$ ⓑ $xx=x$ ⓒ $\bar{\bar{x}}=x$

Sol:

ⓐ

$$\begin{aligned} LHS &= x+x \\ &= (x+x).1 \\ &= (x+x).(x+\bar{x}) \\ &= x+x\bar{x} \\ &= x+0 \\ &= x \\ &= RHS \end{aligned}$$

ⓑ

$$\begin{aligned} LHS &= xx \\ &= xx+0 \\ &= xx+(x.\bar{x}) \\ &= x.(x+\bar{x}) \\ &= x.1 \\ &= x \\ &= RHS \end{aligned}$$

ⓒ

$$\begin{aligned} LHS &= \bar{\bar{x}} \\ &= \bar{\bar{x}}+0 \\ &= \bar{\bar{x}}+x\bar{x} \\ &= [\bar{\bar{x}}+x][\bar{\bar{x}}+\bar{x}] \\ &= (x+\bar{\bar{x}})(\bar{x}+\bar{\bar{x}}) \\ &= (x+\bar{\bar{x}}).1 \end{aligned}$$

$$\begin{aligned} &= (x+\bar{\bar{x}})(x+\bar{x}) \\ &= x+\bar{\bar{x}}.\bar{x} \\ &= x+0 \\ &= x \\ &= RHS \end{aligned}$$

3) For each pair of elements x and y in a Boolean algebra. (a) $x + xy = x$ (b) $x(x+y) = x$

Sol:

(a) $x + xy = x.1 + xy$
$= x(1+y)$
$= x.1$
$= x$
$= RHS$

(b) $LHS = x(x+y)$
$= x.x + x.y$
$= x + x.y$
$= x(1+y)$
$= x.1$
$= x$
$= RHS$

4) For each pair of elements x and y in a Boolean algebra
(a) $x + \bar{x}y = x + y$ (b) $x(\bar{x}+y) = xy$

Sol. (a)
$LHS = x + \bar{x}y$
$= (x+\bar{x})(x+y)$
$= 1.(x+y)$
$= x+y$
$= RHS$

(b) $LHS = x(\bar{x}+y)$
$= x.\bar{x} + xy$
$= 0 + x.y$
$= xy$
$= RHS$

5) For every $x, y \in Z$ in a Boolean algebra
(a) $x + (y+z) = (x+y) + z$ (b) $x(yz) = (xy)z$

Sol: (a)
Let $A = x + (y+z)$ & $B = (x+y) + z$.

Now $xA = xA$ & $xB = xB$
$= x[x + (y+z)]$ $= x[(x+y) + z]$
$= x$ $= x(x+y) + xz$
$= x + xz$
$= x$

$\therefore x A = x B = x \quad -(*)$

Now $\bar{x} A = \bar{x} A$

$= \bar{x}[x + (y+z)]$

$= \bar{x} x + \bar{x}(y+z)$

$= x\bar{x} + \bar{x}(y+z)$

$= 0 + \bar{x}(y+z)$

$= \bar{x}(y+z)$

$\bar{x} B = \bar{x} B$

$= \bar{x}[(x+y) + z]$

$= \bar{x}(x+y) + \bar{x} z$

$= (\bar{x} x + \bar{x} y) + \bar{x} z$

$= (x\bar{x} + \bar{x} y) + \bar{x} z$

$= (0 + \bar{x} y) + \bar{x} z$

$= \bar{x} y + \bar{x} z$

$= \bar{x}(y+z)$

$\therefore \bar{x} A = \bar{x} B = \bar{x}(y+z) \quad -(1)$

Now, $x A + \bar{x} A = x A + \bar{x} A$

$x A + \bar{x} A = x B + \bar{x} B$ [using $(*)$ & (1)]

$A x + A \bar{x} = B x + B \bar{x}$

$A(x + \bar{x}) = B(x + \bar{x})$

$A \cdot 1 = B \cdot 1$

$A = B$

$\Rightarrow \boxed{x + (y+z) = (x+y) + z}$ //

6 For each pair of elements x and y in a Boolean Algebra

(a) $\overline{x+y} = \bar{x}\,\bar{y}$ (b) $\overline{xy} = \bar{x} + \bar{y}$

Rel: Let For every x in a Boolean algebra there is a unique $\bar{x}$ such that $x + \bar{x} = 1$ and $x\bar{x} = 0$

(a) It is sufficient to S.T $\bar{x}\bar{y}$ is the complement of $x+y$. i.e $(x+y) + (\bar{x}\,\bar{y}) = 1$ & $(x+y)(\bar{x}\,\bar{y}) = 0$

Now $(x+y) + (\bar{x}\,\bar{y}) = [(x+y) + \bar{x}\,][(x+y) + \bar{y}]$

$= [(y + x) + \bar{x}][(x + y) + \bar{y}]$

$= [y + (x + \bar{x})][x + (y + \bar{y})]$

$= (y + 1)(x + 1)$

$= 1 \cdot 1$

$= 1$

Also, $(x + y)(\bar{x}\,\bar{y}) = (\bar{x}\,\bar{y})(x + y)$

$= (\bar{x}\,\bar{y})x + (\bar{x}\,\bar{y})y$

$= (\bar{y}\,\bar{x})x + (\bar{x}\,\bar{y})y$

$= \bar{y}(x\bar{x}) + \bar{x}(y\bar{y})$

$= \bar{y} \cdot 0 + \bar{x} \cdot 0$

$= 0 + 0$

$= 0$

(b)

7) Apply Demorgan's theorem to each expression.

ⓐ $\overline{(A+B)+\bar{C}}$ ⓑ $\overline{(\bar{A}+B)+\bar{C}D}$ ⓒ $\overline{(A+B)\bar{C}\bar{D}+E+\bar{F}}$

Sol:

ⓐ $\overline{(A+B)+\bar{C}} = \overline{(A+B)}\cdot\bar{\bar{C}} = (A+B)C$ //

ⓑ $\overline{(\bar{A}+B)+\bar{C}D} = \overline{(\bar{A}+B)}\cdot\overline{\bar{C}D} = (\bar{A}+B)CD$ //

ⓒ $\overline{(A+B)\bar{C}\bar{D}+E+\bar{F}} = \overline{(A+B)\bar{C}\bar{D}}\cdot\bar{E}\cdot\bar{\bar{F}}$

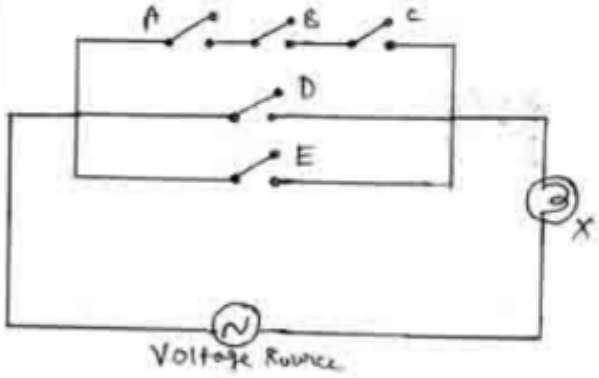
$= [\overline{(A+B)}+\bar{\bar{C}}+\bar{\bar{D}}]\,\bar{E}F$

$= (\bar{A}\bar{B}+C+D)\bar{E}F$

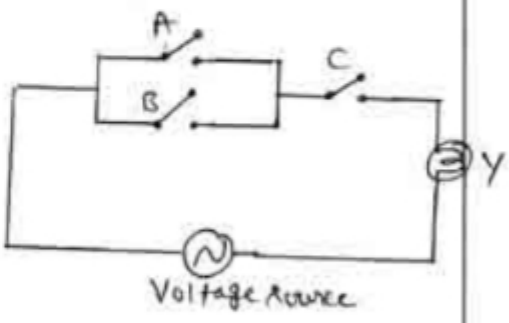
8) Write a switching circuit for the following Boolean expressions ⓐ $X = ABC+D+E$ ⓑ $Y=(A+B)C$

Sol:

ⓐ $X = ABC+D+E$



ⓑ $Y=(A+B)C$



9) Find the complement of the following Boolean functions

ⓐ $X = A(B+C)$ ⓑ $(A+B)(C+D)$

Sol: ⓐ $\bar{X} = \overline{A(B+C)}$

$\Rightarrow \bar{X} = \bar{A}+\overline{B+C}$

$= \bar{A}+\bar{B}\cdot\bar{C}$

ⓑ Let $Y = (A+B)(C+D)$

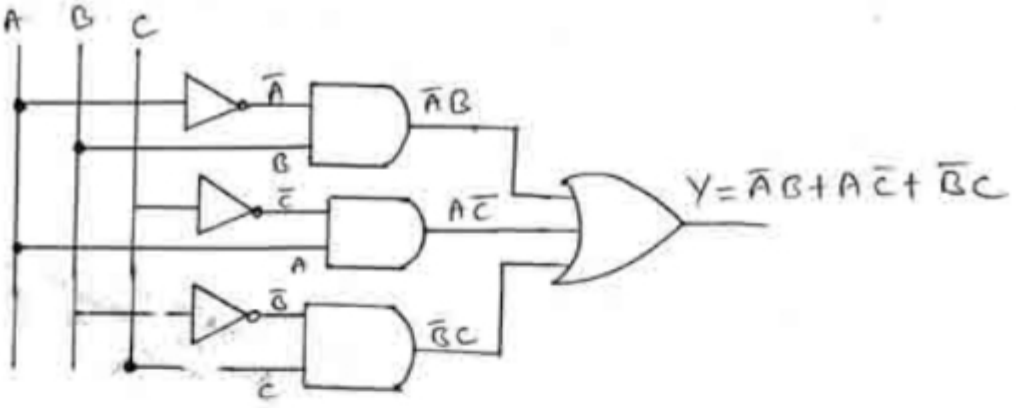
$\Rightarrow \bar{Y} = \overline{(A+B)(C+D)}$

$\bar{Y} = \overline{A+B}+\overline{C+D}$

$= \bar{A}\cdot\bar{B}+\bar{C}\cdot\bar{D}$

(10) Realize the Boolean expression $Y = \bar{A}B + A\bar{C} + \bar{B}C$

Sol:



(11) Implement the function using the truth table shown below. using minimum number of gates.

Inputs			output
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	0	0	1
1	1	1	1

Sol: From the truth table, the output Y is 1 when

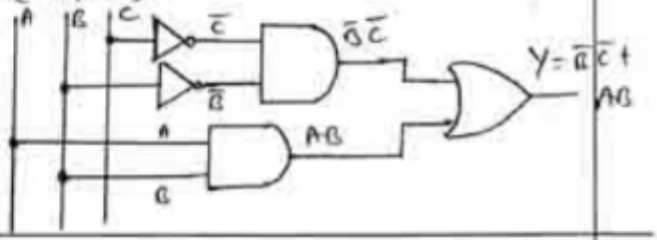
$A = 0, B = 0, C = 0$, $A = 1, B = 0, C = 0$, $A = B = 1, C = 0$ &

$A = B = C = 1$

$\therefore Y = \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + AB\bar{C} + ABC$

$= (\bar{A} + A)\bar{B}\bar{C} + AB(\bar{C} + C)$

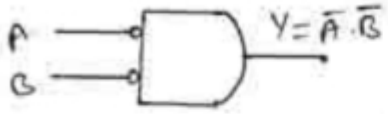
$= \bar{B}\bar{C} + AB$



12) Show that the bubbled AND gate is same as NOR gate:

Sol:

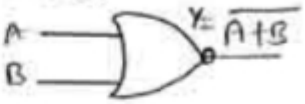
Bubbled AND is shown in fig①



Fig①

Output $\boxed{Y = \bar{A}.\bar{B}}$ // ... -①

NOR gate is shown in fig②



Output

$Y = \overline{\bar{A}+\bar{B}}$

$\boxed{Y = \bar{A}.\bar{B}}$ // -②

From ① & ②, we can conclude that the bubbled AND gate is same as NOR gate

(∵ From De Morgan's law $\overline{\bar{A}+\bar{B}} = \bar{A}.\bar{B}$)

3) Write the Dual of following expressions

ⓐ $A+1=1$ ⓑ $A.1=A$ ⓒ $A+BC=(A+B)+(A+C)$

Sol:

ⓐ Given $A+1=1$

Dual of $A+1=1$ is

$\boxed{A.0=0}$ //

ⓑ Given $A.1=A$

Dual of $A.1=A$ is

$\boxed{A+0=A}$ //

ⓒ Given

$A+BC=(A+B)+(A+C)$

Dual of $A+BC=(A+B)+(A+C)$ is

$\boxed{A(B+C)=(AB)(AC)}$ //

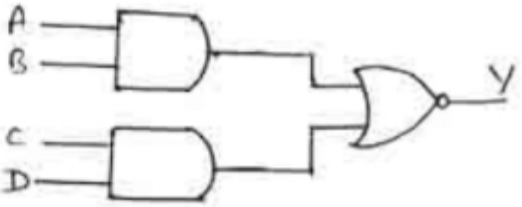
Hint: ① Replace AND to OR & OR to AND (. to +) (+ to .)

② Replace 1 to 0 & 0 to 1

4) Draw AND-OR-Invert (AOI) circuit & write the output expression

Sol:

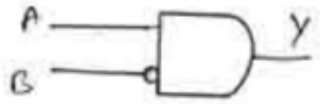
$Y = \overline{AB+CD}$



(15) Explain inhibit & Enable operation for
(a) Two input AND gate (b) Two input AND gate with strobe

Sol.

(a)



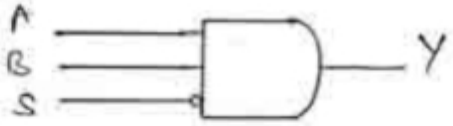
output is,

$Y = A\bar{B}$

If $B=0$, $Y=1$ (Enable)
& $A=1$

If $S=1$, $Y=0$, (inhibit)

(b)

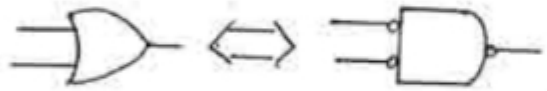


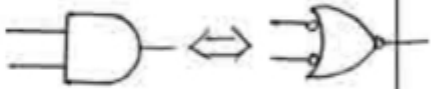
output, $Y = AB\bar{S}$

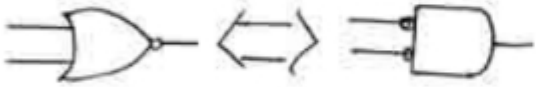
If $A=1$, $B=1$, $S=0$, then $Y=1$, then gate is enabled

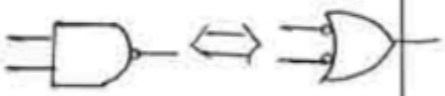
If $A=1$ @ 0, $B=1$ @ 0, $S=1$, the output $Y=0$, then the gate is inhibited

(16) Prove the following equalities.

(a) 

(b) 

(c) 

(d) 

Sol: Let A, B be inputs, Y be output

(a) $Y = A+B = \overline{\bar{A}\cdot\bar{B}} = \bar{\bar{A}}+\bar{\bar{B}} = A+B$

(b) $Y = AB = \overline{\bar{A}+\bar{B}} = \bar{\bar{A}}\cdot\bar{\bar{B}} = AB$

(c) $Y = \overline{A+B} = \bar{A}\cdot\bar{B}$

(d) $Y = \overline{A\cdot B} = \bar{A}+\bar{B}$

[DeMorgan's theorem
$\overline{A+B} = \bar{A}\cdot\bar{B}$
$\overline{A\cdot B} = \bar{A}+\bar{B}$]

(17) Simplify the following

(a) $XY + X'Z + YZ$

(b) $\overline{\bar{A}(B+\bar{C})}(A+\bar{B}+C)(\overline{\bar{A}\bar{B}\bar{C}})$

(c) $\overline{(A+B)(A+C+\bar{D})(A+\bar{C}+D)(B+\bar{C})}$

(d) $(B+\bar{C})(\bar{B}+C)(\overline{\bar{A}+B+\bar{C}})$

Ans:

(a) Let $A = XY + X'Z + YZ$ (Here $X' = \bar{X}$)

$= XY + X'Z + YZ(X + X')$ $(\because X + X' = 1)$

$= XY + X'Z + XYZ + X'YZ$

$= XY(1 + Z) + X'Z(1 + Y)$

$= XY + X'Z$

(b) Let $X = \overline{\bar{A}(B + \bar{C})} \cdot (A + \bar{B} + C)\overline{(\bar{A}\,\bar{B} \cdot \bar{C})}$

$= (\bar{\bar{A}}) + (\overline{B + \bar{C}})(A + \bar{B} + C)(\bar{\bar{A}} + \bar{\bar{B}} + \bar{\bar{C}})$

$= (A + \bar{B} \cdot \bar{\bar{C}})(A + \bar{B} + C)(A + B + C)$

$= (A + \bar{B}C)(A + \bar{B} + C)(A + B + C)$

$= (AA + A\bar{B} + AC + A\bar{B}C + \bar{B}\bar{B}C + \bar{B}CC)(A + B + C)$

$= (A + A\bar{B} + AC + A\bar{B}C + \bar{B}C + \bar{B}C)(A + B + C)$

$= (A(1 + \bar{B} + \bar{C} + \bar{B}C) + \bar{B}C)(A + B + C)$

$= (A + \bar{B}C)(A + B + C)$

$= AA + AB + AC + A\bar{B}C + B\bar{B}C + \bar{B}CC$

$= A + AB + AC + A\bar{B}C + \bar{B}C$

$= A(1 + B + C + \bar{B}C) + \bar{B}C$

$= A + \bar{B}C$

(c) Let $Y = (A + B)(A + C + \bar{D})(A + \bar{C} + D)(B + \bar{C})$

$= (AA + AC + A\bar{D} + AB + BC + B\bar{D})$ $[AA = A,\ \bar{C}\bar{C} = \bar{C}]$

$(AB + A\bar{C} + B\bar{C} + \bar{C}\bar{C} + BD + \bar{C}D)$

$= (A + AC + A\bar{D} + AB + BC + B\bar{D})(AB + A\bar{C} + B\bar{C} + \bar{C} + BD + \bar{C}D)$

$= [A(1 + C + \bar{D} + B) + BC + B\bar{D}][AB + \bar{C}(A + B + 1 + D) + BD]$

$= [A + BC + B\bar{D}][AB + \bar{C} + BD]$

$= AAB + A\bar{C} + ABD + ABBC + B\bar{C}\bar{C} + BBCD + ABB\bar{D} + B\bar{C}\bar{D} + BB\bar{D}\bar{D}$

$AB + A\bar{C} + ABD + ABC + BCD + AB\bar{D} + B\bar{C}\bar{D}$

$= [AB(1 + D + \bar{C} + \bar{D}) + A\bar{C} + BCD + B\bar{C}\bar{D}]$

$= AB + A\bar{C} + BCD + B\bar{C}\bar{D}$

$= A(B + \bar{C}) + B(CD + \bar{C}\bar{D})$ //

(d) Let

$Y = \overline{(B + \bar{C})(\bar{B} + C)(\bar{A} + B + \bar{C})}$

$= \overline{(B\bar{B} + BC + \bar{B}\bar{C} + C\bar{C})(\bar{A} \cdot \bar{B} \cdot \bar{C})}$

$= \overline{(BC + \bar{B}\bar{C})(A\bar{B}C)}$

$= \overline{AB\bar{B}CC + A\bar{B}\bar{B}C\bar{C}}$

$= \overline{0}$

$= 1$ //

(or) $Y = \overline{(B + \bar{C})(\bar{B} + C)(\bar{A} + B + \bar{C})}$

$= \overline{(B + \bar{C})} + \overline{(\bar{B} + C)} + \overline{(\bar{A} + B + \bar{C})}$

$= (\bar{B} \cdot C) + (B \cdot \bar{C}) + (\bar{A} + B + \bar{C})$

$= \bar{B}C + B\bar{C} + \bar{A} + B + \bar{C}$

$= \bar{B}C + B(\bar{C} + 1) + \bar{A} + \bar{C}$

$= \bar{B}C + B + \bar{A} + \bar{C}$

$= B + C + \bar{A} + \bar{C} = B + \bar{A} + \bar{C} + C$

$= B + \bar{A} + 1$

$= 1$ //

Syllabus: Introduction to Flip-Flops, NAND Gate Latch/ NOR Gate Latch, RS Flip-Flop, Gated Flip-Flops: Clocked RS Flip-Flop.

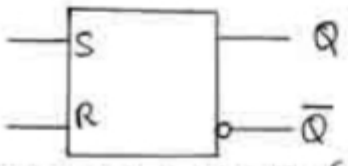
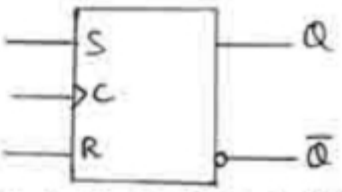
* Introduction:

Latch: Latch is a bistable element, whose output changes when its input change.

Flip-Flop: Flip-Flop is a bistable element, whose output changes only either at the rising (or) falling edge of the enable signal (clock signal)

Note:

① Comparision of Latch & Flip-Flop:

Latch	Flip-Flop (Bistable multivibrator)
① Latch is a bistable element, whose output changes when its input changes (Sometime clock signal may be present)	① Flip-Flop is a bistable element, whose output changes only either at the rising (or) falling edge of the enable signal (clock signal)
② It doesnot require any extenal timing signals (Asynchronous device)	② It require special timing signal called the clock (Synchronous device)
③ Output changes when its input changes	③ Its content (output) remains constant even if the input changes
④ Symbol of Latch is shown in fig①  Active-high input S-R Latch (Fig①)	④ Symbol of Flip-Flop is shown in fig②  Positive edge triggered SR FF (Fig②)

(5) The input lines are continuously being interrogated	(5) Inputs are normally sampled & not interrogated continuously.
(6) It is the basic element for storing information (can store one bit of information)	(6) It is the basic element for storing information (can store one bit of information)

(2) IEEE Logic Symbols & Traditional Logic-gate Symbols

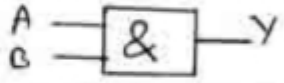
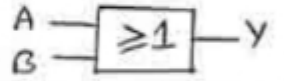
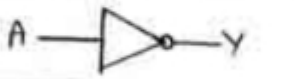
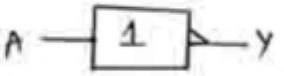
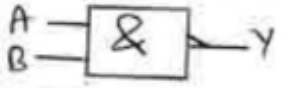
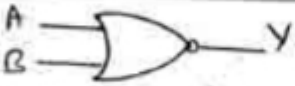
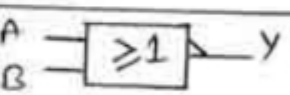
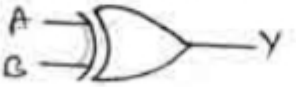
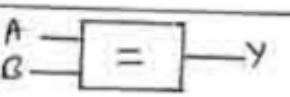
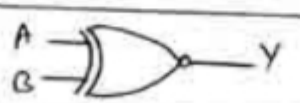
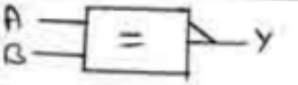
Logic function	Traditional Logic Symbol	IEEE Logic Symbol
AND		
OR		
NOT		
NAND		
NOR		
XOR		
XNOR		

Table (3)

(3) Two categories of Flip-Flops:

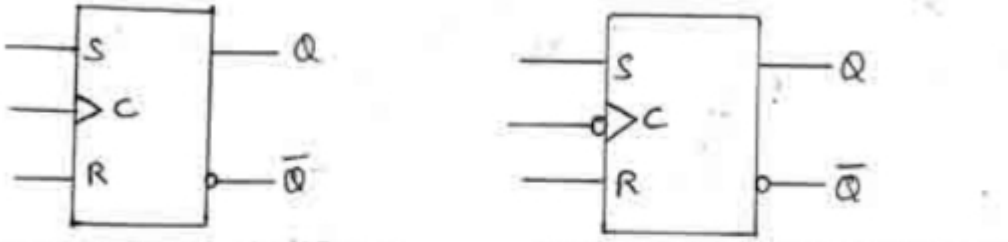
(a) Edge-Triggered Flip-Flops

The term edge-triggered means that the flip-flop changes state either at the positive edge (rising edge)

(a) at the negative edge (falling edge) of the clock pulse & is sensitive to its inputs only at this transition of the clock.

Three basic types of edge-triggered flip-flops:
(i) S-R (ii) D & (iii) J-K.

The logic symbol is shown in fig(4)



(a) Positive edge-triggered (b) negative edge-triggered

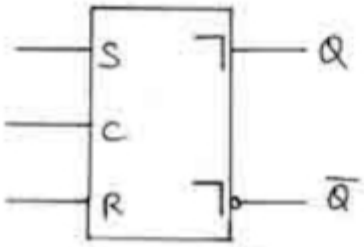
Fig(4): Edge-triggered flip-flop

(b) Pulse-Triggered (Master-Slave) Flip-Flops

The term pulse-triggered means that data are entered into the flip-flop on the leading edge of the clock pulse, but the output doesnot reflect the input state until the trailing edge of the clock pulse. The inputs must be setup prior to the clock pulse's leading edge, but the output is postponed until the trailing edge of the clock.

Three basic types of pulse-triggered flip-flops:
(i) S-R (ii) D & (iii) J-K.

The logic symbol is shown in fig(5)



Fig(5): Pulse-triggered (master slave) flip-flop

* SR Latch @ RS Latch

The simplest type of Latch is SR Latch. It has 2 inputs, namely SET (S) & RESET (R), and 2 outputs Q and $\bar{Q}$.

The SR Latch can be implemented using NAND gates @ NOR gates

(a) NAND Gate Latch @ SR Latch using NAND gates @ RS Latch using NAND gates :

The NAND gate based SR Latch is shown in fig (6)(a). It consists of cross connected NAND gates.

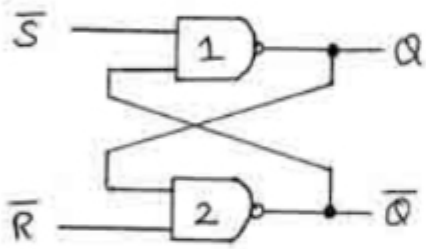


Fig 6(a) : Circuit diagram

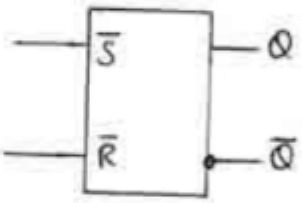


Fig 6(b)

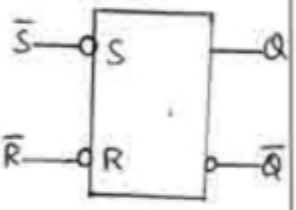


Fig 6(c)

The logic Symbol of SR Latch is shown in fig 6(b).
The IEEE Symbol of SR Latch is shown in fig 6(c).

Operation :

Case 1: $\bar{S}=1, \bar{R}=1$

(a) Let $Q=1$ ($\bar{Q}=0$): The inputs to the gate 1 are $\bar{S}=1$ & $\bar{Q}=0$, So its output is $Q=1$ (No change)
The inputs to the gate 2 are $\bar{R}=1$ & $Q=1$, So its output is $\bar{Q}=0$ (No change)

(b) Let $Q=0$ ($\bar{Q}=1$): The inputs to the gate 1 are $\bar{S}=1$ & $\bar{Q}=1$, So its output is $Q=0$ (No change)
The inputs to the gate 2 are $\bar{R}=1$ & $Q=0$. So its

Output is $\bar{Q}=1$ (No change)

∴ When $\bar{R}=1$, $\bar{S}=1$, the output remains in the previous state (Last state) or output does not change.

Case 2: $\bar{S}=0$, $\bar{R}=1$

(a) Let $Q=1$ ($\bar{Q}=0$): The inputs to the gate 1 are $\bar{S}=0$ & $\bar{Q}=0$, So its output is $Q=1$.

The inputs to the gate 2 are $\bar{R}=1$ & $Q=1$, So its output is $\bar{Q}=0$.

(or)

The input to gate 1 is $\bar{S}=0$, So its output is $Q=1$. Now inputs to the gate-2 are $\bar{R}=1$ & $Q=1$, So its output is $\bar{Q}=0$.

(b) Let $Q=0$ ($\bar{Q}=1$): The inputs to the gate 1 are $\bar{S}=0$ & $\bar{Q}=1$, So its output is $Q=1$

The inputs to the gate 2 are $\bar{R}=1$ & $Q=1$, So its output is $\bar{Q}=0$

∴ When $\bar{S}=0$, $\bar{R}=1$, the output is Set ($Q=1$)

Case 3: $\bar{S}=1$, $\bar{R}=0$

The input to gate 2 is $\bar{R}=0$, So its output is $\bar{Q}=1$. Now inputs to the gate-1 are $\bar{S}=1$ & $\bar{Q}=1$, So its output is $Q=0$.

∴ When $\bar{S}=1$, $\bar{R}=0$, the output is Reset ($Q=0$)

Case 4: $\bar{S}=0$, $\bar{R}=0$

When $\bar{S}=0$, $\bar{R}=0$, both the outputs Q & $\bar{Q}$ try to become 1, which is not possible.

The Condition $\bar{S}=\bar{R}=0$ is avoided because it results in an invalid mode of operation (Forbidden state) [Major drawback

of any SET-RESET type of Latch]

The truth table of NAND gate Latch is shown in fig 6(d)

Inputs		outputs		Comments
$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$	
1	1	NC	NC	No change. Latch remains in previous state
0	1	1	0	Latch SETS
1	0	0	1	Latch RESETS
0	0	1	1	Invalid condition

Fig 6(d)

(b) NOR Gate Latch (a) SR Latch using NOR gates (or) RS Latch using NOR gates :

The NOR gate based SR Latch is shown in fig 7(a)

It consists of cross connected NOR gates

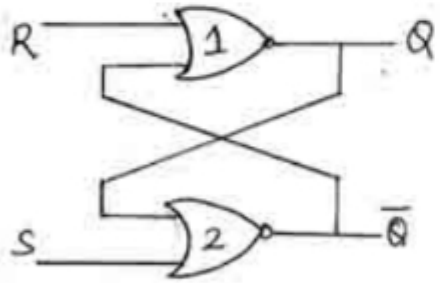


Fig 7(a): circuit diagram

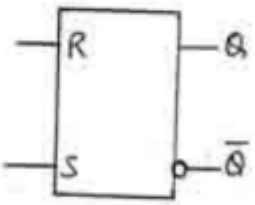


Fig 7(b)

The logic symbol of SR Latch is shown in fig 7(b)

Operation;

Case 1: R=0, S=0

(a) Let Q=1 ($\bar{Q}$=0) : The inputs to the gate 1 are R=0 & $\bar{Q}$=0, So its output is Q=1 (No change)

The inputs to the gate 2 are S=0 & Q=1, So its output

is $\bar{Q}=0$ (No change)

(b) Let $Q=0$ ($\bar{Q}=1$): The inputs to the gate 1 are $R=0$ & $\bar{Q}=1$, So its output is $Q=0$ (No change)

The inputs to the gate 2 are $S=0$ & $Q=0$, So its output is $\bar{Q}=1$ (No change)

∴ When $R=S=0$, the output remains in the previous state.

Case 2: $R=0, S=1$

The input to gate 2 is $S=1$, So its output is $\bar{Q}=0$. Now inputs to gate 1 are $R=0$ & $\bar{Q}=0$. So its output is $Q=1$.

∴ When $R=0, S=1$, the output is Set ($Q=1$)

Case 3: $R=1, S=0$

The input to gate 1 is $R=1$, So its output is $Q=0$. Now inputs to gate 2 are $S=0$ & $Q=0$. So its output is $\bar{Q}=1$.

∴ When $R=1, S=0$, the output is Reset ($Q=0$)

Case 4: $R=1, S=1$

When $R=S=1$, both the outputs Q & $\bar{Q}$ try to become 0, which is not possible.

The condition $R=S=1$, is avoided because it results in an invalid mode of operation (Forbidden State).

The truth table of NOR gate Latch is shown in fig 7©

Inputs		outputs		Comments
R	S	Q	$\bar{Q}$	
0	0	NC	NC	No change. Latch remains in Previous State
0	1	1	0	Latch SETS
1	0	0	1	Latch RESETS
1	1	0	0	Invalid Condition

Fig 7©

Note:

① The outputs $Q/\bar{Q}$ can also be denoted by $X/\bar{X}$ or $A/\bar{A}$

② Q is Normal FF output, $\bar{Q}$ is inverted FF output.

③ $Q=1, \bar{Q}=0$ → SET State or 1 State or High State.

④ $Q=0, \bar{Q}=1$ → LOW State or 0 State or CLEAR or RESET State

⑤ In NAND gate SR Latch, instead of $\bar{S}$ & $\bar{R}$ (inputs), S & R can be used. But in NOR gate SR Latch, instead of S & R, $\bar{S}$ & $\bar{R}$ can be used.

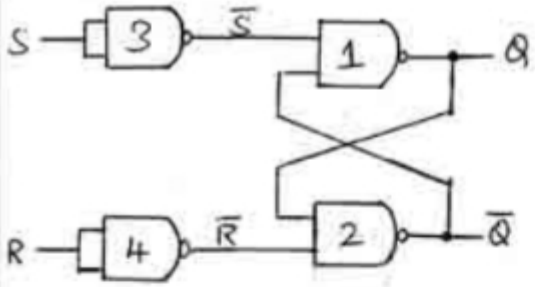
⑥ Sometimes NAND gate based SR Latch is called as $\bar{S}\bar{R}$ Latch (because inputs are $\bar{S}$ & $\bar{R}$)

⑦ RS Flip-Flop or RS Flip-flop Latch or NAND Gate SR Latch

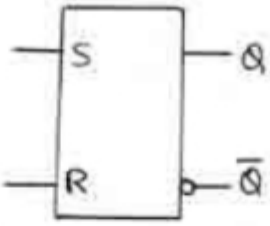
Fig ⑧ shows RS Flip-flop (alternative way of NAND Gate SR Latch implementation)

Explanation is same as NAND Gate SR Latch (page 4)

Case 1: $\bar{S}=1, \bar{R}=1$ ($\Leftrightarrow S=0, R=0$)



(a) Circuit diagram of RS flip-flop latch



(b) Logic Symbol

Inputs		Outputs		Comments
S	R	Q	$\bar{Q}$	
0	0	NC	NC	Last State (or) No change (or) Previous State
1	0	1	0	SET
0	1	0	1	RESET
1	1	1	1	Invalid condition (forbidden)

(c) Truth table

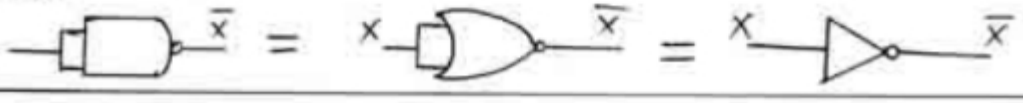
Fig (a) : RS-Flip-flop

Case 2: $\bar{S}=0$, $\bar{R}=1$ ($\Rightarrow S=1, R=0$)

Case 3: $\bar{S}=1$, $\bar{R}=0$ ($\Rightarrow S=0, R=1$)

Case 4: $\bar{S}=0$; $\bar{R}=0$ ($\Rightarrow S=1, R=1$)

Gates (3) & (4) can be replaced by NOT gates (or) NOR gates.



Gated Flip-flops (Clocked RS Flip-flops) (Enable RS FFs)

Clocked RS Flip-flop using NAND gates

The Clocked RS NAND gate flip-flop is shown in fig 9(a)

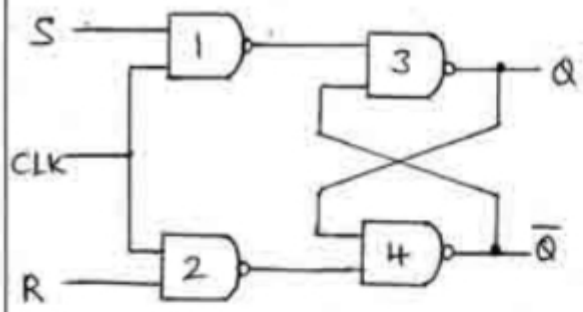


Fig 9(a): circuit diagram

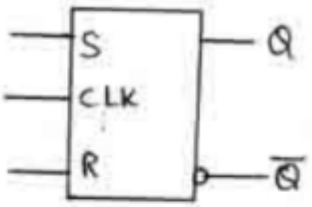


Fig 9(b): Logic Symbol

The logic Symbol of clocked RS NAND gate flip-flop is shown in fig 9(b).

Operation:

- **Clock is Low (CLK = 0):**

When the clock is low, the output of gates 1 and 2 is high(1). Hence the output of gates 3 & 4 will not change regardless of S & R input values.

∴ When CLK = 0, S = X, R = X, the output remains in the previous state.

- **Clock is high (CLK = 1):**

Case 1: S = 0, R = 0

When R = S = 0 (CLK = 1), the output remains in the previous state.

Case 2: S = 1, R = 0

When S = 1, R = 0 & CLK = 1, the output is Set (Q = 1)

Case 3: S = 0, R = 1

When S = 0, R = 1 & CLK = 1, the output is Reset (Q = 0)

Case 4: S = 1, R = 1

When S = R = CLK = 1, both the outputs Q & $\overline{Q}$ try to

become 1, which is not possible (Invalid condition or Forbidden state)

The truth table of clocked RS NAND gate flip-flop is shown in fig 9©.

Inputs			outputs		Comments
CLK	S	R	Q	$\overline{Q}$	
0	X	X	NC	NC	No change (previous state)
1	0	0	NC	NC	No change (Previous state)
1	1	0	1	0	SET
1	0	1	0	1	RESET
1	1	1	1	1	Invalid

Fig 9© : Truth table of clocked RS NAND gate FF

b) Clocked RS Flip-flop using NOR gates

The clocked RS NOR gate flip-flop is shown in fig 10@

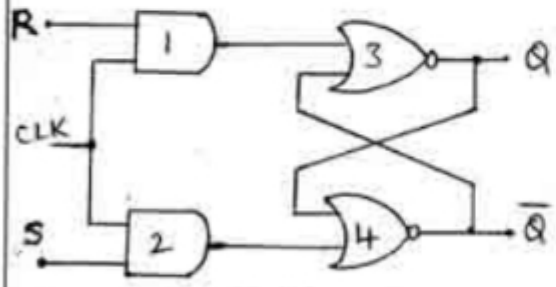


Fig 10@ : Circuit diagram

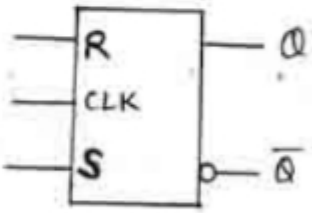


Fig 10ⓑ: Logic Symbol

The logic Symbol of clocked RS NOR gate flip-flop is shown in fig 10ⓑ.

Operation:

- Clock is Low (CLK=0):

When the clock is low, the output of gates 1 and 2 is Low(0). Hence the output of gates 3 & 4 will not change regardless of S & R input values.

∴ When CLK = 0, S = X, R = X, the output remains in the previous state.

- Clock is high (CLK = 1):

Case 1: R = 0, S = 0

When R = S = 0 & CLK = 1, the output remains in the previous state.

Case 2: R = 0, S = 1

When R = 0, S = 1 & CLK = 1, the output is Set (Q = 1)

Case 3: R = 1, S = 0

When R = 1, S = 0 & CLK = 1, the output is Reset (Q = 0)

Case 4: R = 1, S = 1

When R = S = CLK = 1, both the outputs Q & $\bar{Q}$ try to become 0, which is not possible (Invalid Condition @ Forbidden state)

The truth table of Clocked RS NOR gate flip-flop is shown in fig 10©

Inputs			Outputs		Comments
CLK	R	S	Q	$\bar{Q}$	
0	X	X	NC	NC	No change (previous state)
1	0	0	NC	NC	No change (previous state)
1	0	1	1	0	SET
1	1	0	0	1	RESET
1	1	1	0	0	Invalid Condition

Fig 10©: Truth table of clocked RS NOR gate FF

Note: X → Don't care (1 or 0)

Problems

① If the $\bar{S}$ & $\bar{R}$ waveforms in fig 1@ are applied to the inputs of the Latch of fig 1⑥, determine the waveform that would be observed on the Q output. Assume that Q is initially Low.

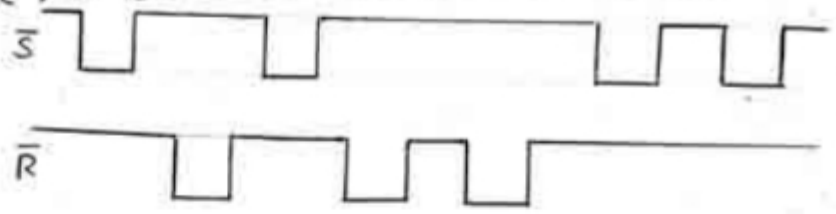


Fig 1@

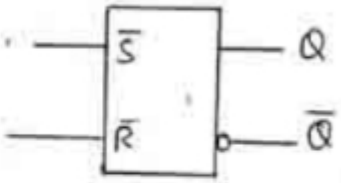
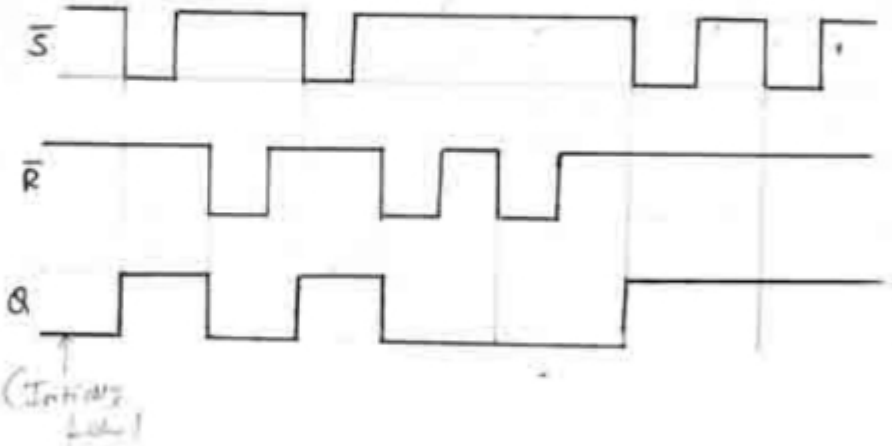


Fig 1⑥

Sol: We have truth table of SR Latch

Inputs		o/p
$\bar{S}$	$\bar{R}$	Q
1	1	NC
0	1	1
1	0	0
0	0	1



② Construct the TT for the circuit shown in fig ②

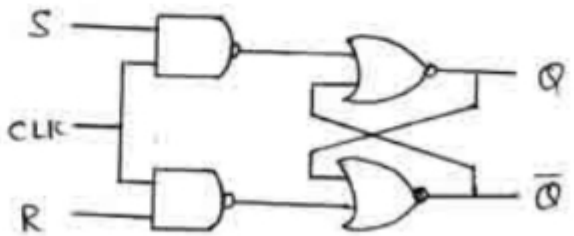
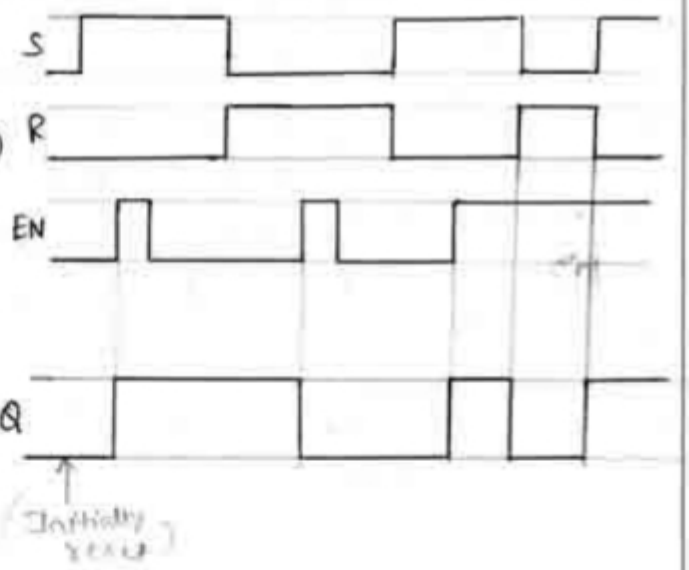


Fig ②

Sol:

Inputs			outputs		
CLK	S	R	Q	$\bar{Q}$	
0	X	X	0	0	} Invalid
1	0	0	0	0	
1	0	1	0	1	→ Reset
1	1	0	1	0	→ Set
1	1	1	NC	NC	} Previous State

3) Determine the Q-output waveform if the inputs shown in fig 3(a) are applied to a gated S-R latch that is initially RESET



(a)

d:

Inputs			output
CLK	S	R	Q
0	X	X	Q (NC)
1	0	0	Q (NC)
1	1	0	1
1	0	1	0
1	1	1	Invalid (Avoided)

Syllabus: Introduction to microcontroller, 8051 microcontroller Architecture and an example of microcontroller based Stepper motor control system (only Block diagram approach)

* Introduction:

→ In 1981, Intel Corporation introduced an 8-bit microcontroller, called the 8051.

→ Some of the companies producing a member of the 8051 family: Intel, Atmel, Philips/ Signetics, Infincon, Dallas Semi / Maxim, Motorola etc

→ A microcontroller has a CPU (a microprocessor) in addition to a fixed amount of RAM, ROM, I/o ports, & a timer all on a single chip.

The processor, RAM, ROM, I/o ports, & timer are all embedded together on a single chip it a microcontroller

→ Advantages of microcontroller (MC)

① No need of any external memory, I/o & timer.
② Higher Performance
③ Lower Power Consumption
④ Compact Size

→ Criteria for Choosing a microcontroller

① Speed
② Packaging
③ Power Consumption
④ Cost / unit
⑤ Amount of RAM & ROM on chip
⑥ Number of I/o pins & the timer on the chip
⑦ Ease of upgrading to higher-Performance ⑧ Lower Power Consumption versions.

→ Applications of Microcontroller

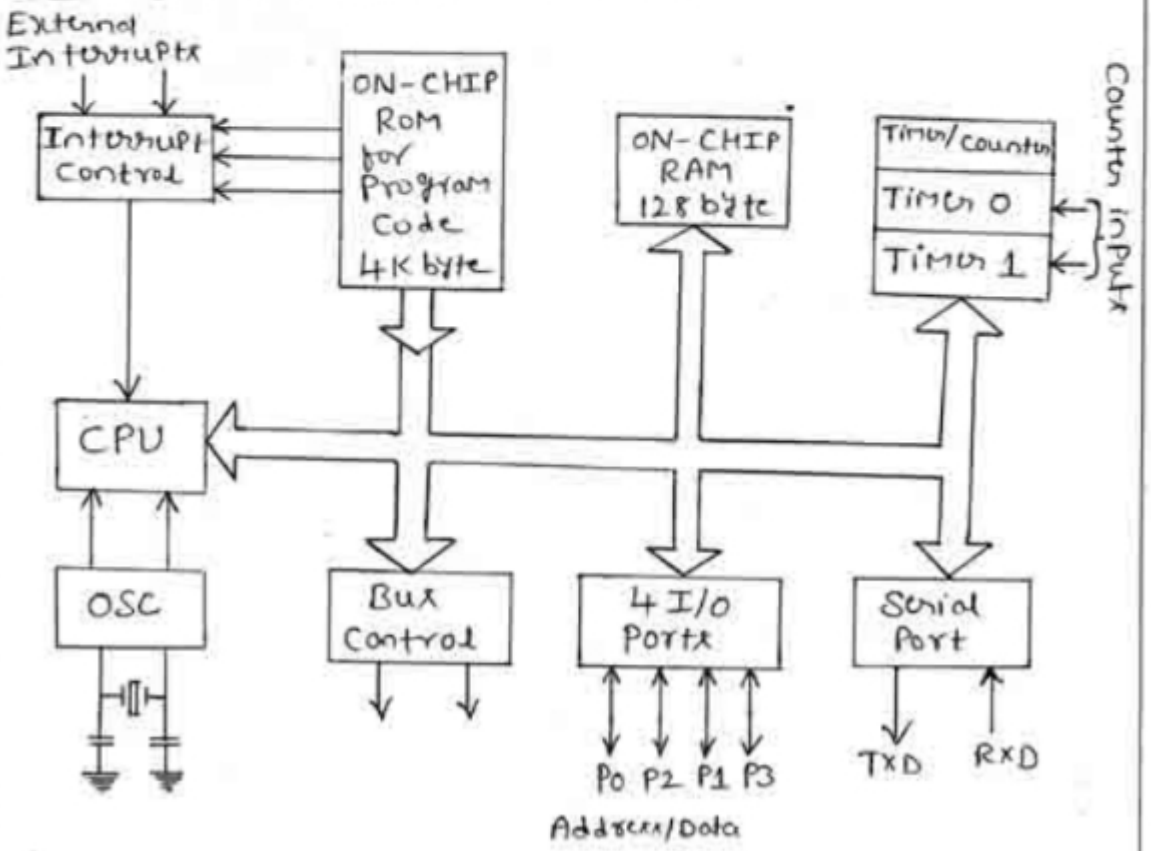
Home appliances	Office	Others
① Intercom	① Telephones	① Engine control
② Telephones	② Computers	② Air bag
③ Security Systems	③ Copiers	③ Climate control
④ Fax Machines	④ Laser Printer	④ Keyless entry
⑤ Computers	⑤ Color Printer	⑤ Instrumentation
⑥ Camcorder	⑥ Network Server	⑥ Cars
⑦ Remote Controls	⑦ Internet terminal	⑦ Traffic Signals
⑧ VCR	⑧ Mouse	⑧ Aerospace
⑨ Video games	⑨ CD-ROM drives	⑨ Diagnostics
⑩ Camera	⑩ Elevators	⑩ Water level controllers.
⑪ Paging	⑪ Modem	
⑫ Sewing Machines		
⑬ Musical Instruments		
⑭ Cellular Phones		
⑮ Cable TV tuner		
⑯ TVs		
⑰ Washing Machines		

→ Features of 8051 Microcontroller

① 8-bit CPU
② 128 bytes of RAM.
③ 4K bytes of on-chip ROM. (8051 can have a maximum of 64K bytes of on-chip ROM)
④ Two 16 bit timers/Counters
⑤ One Serial Port
⑥ Four I/o ports (each 8-bits wide) (Provides 32 I/o Pins)

⑦ 8-bit Program Status Word (PSW)
⑧ 16-bit Program counter (PC) and data Pointer (DPTR)
⑨ 8-bit Stack Pointer (SP)
⑩ Two external & three internal interrupts
⑪ Four register banks, each containing 8 registers.
⑫ 8-bit data bus
⑬ 16-bit address bus.
⑭ Full duplex Serial data transmitter/ receiver
⑮ Oscillator & Clock circuits (Operates at a clock frequency of 12MHz)

* Block diagram of 8051 microcontroller (07)
Architecture of 8051 Microcontroller



Fig①: Block diagram of 8051 microcontroller

The block diagram of 8051 microcontroller is shown in fig①.

8051 microcontroller consists of Registers, memory, I/o ports, Interrupts, Timer/Counters, UART, Oscillator & clock circuits.

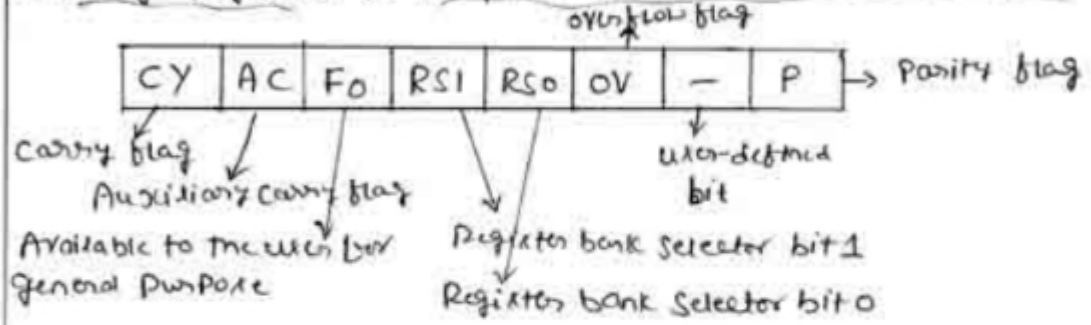
* A register (Accumulator): It is an 8-bit register used for arithmetic & logical operations.
* B register: It is an 8-bit register used for multiplication & division operations.
* Internal memory: Internal memory of 8051 are
  ⓐ 128 bytes RAM ⓑ 128 bytes of Special function RAM
  ⓒ 4K bytes ROM.
* External memory: External memory of 8051 are
  ⓐ ROM (64K bytes for program)
  ⓑ RAM (64K bytes of data memory)
* Stack: It is a section of internal RAM used to store information temporarily (data & address)
* Stack Pointer (SP): It is an 8-bit register used to access the stack
* I/o Ports: There are four I/o ports each comprising 8 bits, namely P0, P1, P2 & P3

  Three types of buses are used
  ⓐ Address Bus (16-bit) ⓑ Data Bus (8 bit bi-directional)
  ⓒ control Bus (consists of RD, WR, PSEN, ALE & EA)
* DPTR (Data Pointer): It is a 16-bit register used to hold the address of external data memory & program memory. It consists of two 8-bit registers namely DPH (high byte) & DPL (Low byte)
* Program counter (PC): It is a 16-bit register which holds

ⓐ Instruction Pointer (IP)

the address of the next instruction to be executed

- **Interrupts**: There are six interrupts in the 8051.
- **Timers/counters**: 8051 has two timers/counters: Timer0 & Timer1 (16-bits)
- **Register banks**: There are four register banks each consisting of 8-bit general purpose registers ($R_0 - R_7$)
- **Flag register & Program Status Word (PSW) register**:



- **UART (Universal Asynchronous receiver & transmitter)**: It is used for sending & receiving data bits serially.
- **Oscillator & clock circuits**: Operates at a clock frequency of 12MHz.

Microcontroller based Stepper motor control System

8051 microcontroller connection to the Stepper motor:

The microcontroller based Stepper motor control System is shown in fig ②.

It consists of 8051 microcontroller, resistors, ULN 2003 & a Stepper motor.

8051 microcontroller:

- 8051 MC is low Power, high-Performance, 8-bit Processor.

Resistors:

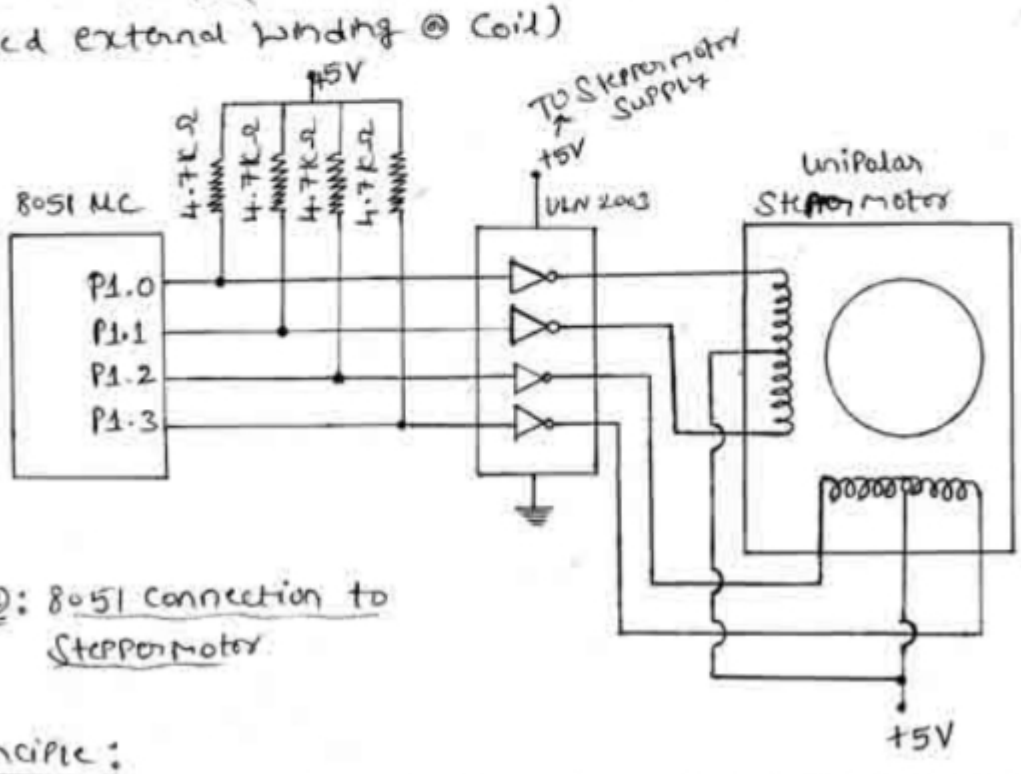
- If it is required, the external pull up resistors are connected to pins depending on the microcontroller.

ULN 2003:

- It is a high voltage & high current darlington array IC.

Stepper motor:

- It is an electromechanical device which converts electrical pulses into mechanical motion.
- This motor divides the complete rotation (360°) into a number of equal steps.
- Stepper motor consists of a rotor (rotating shaft (motor shaft (usually a permanent magnet) & a stator (fixed external winding (coil)



Fig②: 8051 connection to stepper motor

Principle:

- The main principle of the circuit is to rotate the stepper motor stepwise at a particular step angle.

- The speed of the motor is determined by the time delay between each incremental movement.
- motor moves each time a pulse is received.
- The stepper motor has 4 coils. These four coils are activated in the cyclic order methods
  - (a) Full step drive : Two coils are energized at a time.
  - (b) Half step drive : coils are energized alternatively
- Motor is connected to the Port 1 (P1.0 – P1.3) of the microcontroller through a driver IC
- The ULN 2003 IC is used to drive the stepper motor as the controller cannot provide current required by the motor (Stepper motor requires more than 60mA)
- Table ③ shows a 2-phase, 4-step stepping sequence

Step #	Winding A	Winding B	Winding C	Winding D
1	1	0	0	1
2	1	1	0	0
3	0	1	1	0
4	0	0	1	1

clockwise ↓ counter clockwise ↑

Table ③: Normal 4-Step Sequence

* Step angle (degrees) $\text{Step angle} = \frac{360}{\text{No of steps per revolution}}$
* Revolutions Per minute (RPM) $\text{RPM} = \frac{60 \times \text{Steps per second}}{\text{Steps per revolution}}$
* Advantages: • High resolution dynamic torque

- Requires low operating voltage
- Consumes less power
- cost-effective
- No encoder is required for simple positioning etc

*Applications:

- Facsimile machines • Plotters • Image Scanners
- Copiers • Robotics • Dot matrix printers • Clocks
- Card readers • floppy disk • hard disk drives
- tele printers • teletype

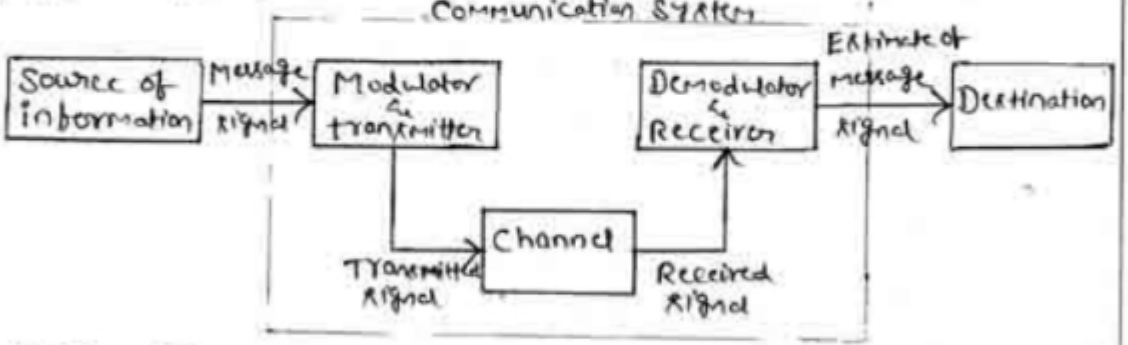
Syllabus: Introduction, Elements of Communication Systems, Modulation: Amplitude Modulation, Spectrum Power, AM Detection (Demodulation), Frequency and Phase Modulation. Amplitude and Frequency Modulation: A Comparision.

* **Communication:** Communication is the process of exchanging information between two points (through connection (Wired) & connectionless (Wireless) medium)

* **Communication System:** Communication system is a set of electronic equipments used for communication purpose.

* **Elements of Communication Systems (Block diagram of Communication System):**

Fig① shows the basic elements of a communication system



Fig①: Block diagram of Communication System

Source of information:

→ The four important sources of information are:
ⓐ Speech ⓑ Television ⓒ Facsimile (Fax) & ⓓ Personal computers

→ The signal that carries information cannot travel long distance.

Modulator & transmitter:

→ It converts the information signal to a form suitable

for transmission over the channel (Modulation)
→ It amplify the information signal.

Channel:

→ It is the physical medium through which the information is sent. (It may introduce noise & distortion)
→ It can be a pair of conducting wires, optical fiber, co-axial cable, waveguide & free space.

Demodulator & Receiver:

→ It extracts the message signal from the received signal (Demodulation & Detection)
→ It amplify the message signal. (& filtering → Remove noise)

Destination:

→ The message signal is fed to Loud speakers, TV picture tube, Computer display screens etc

Note:

① Message signal is called as Information signal & Baseband signal & Unmodulated signal & Low frequency signal & Modulating signal

② Carrier signal is called as High frequency signal.

③ Frequency range with application

Sl no.	Frequency range (Band)	Applications
1	30Hz - 300Hz, Extremely Low frequencies (ELF)	Power transmission
2	300Hz - 3KHz, Voice frequency (VF)	Audio, Submarine communication, Navigation

3	3KHz - 30KHz, Very Low frequencies (VLF)	Submarine Communication, Navigation
4	30KHz - 300KHz, Low frequencies (LF)	Submarine Communication, Navigation.
5	300KHz - 3MHz, Medium frequencies (MF)	AM broadcast, Aeronautical Comm.
6	3MHz - 30MHz, High frequencies (HF)	Shortwave transmission.
7	30MHz - 300MHz, Very high frequencies (VHF)	TV & FM broadcast.
8	300MHz - 3GHz, ultra high frequencies (UHF)	Communication Satellite, Cellular Phones, Personal Com. System
9	3GHz - 30GHz, Super high frequencies (SHF)	Satellite communication, Radar
10	30GHz - 300GHz, Extremely high freq (EHF)	Satellite Communication, Radar

* Need for modulation:

① Increases the operating range ② Increases the range of communication ③ Long distance communication:

Modulation increases the frequency of the signal & thus they can be transmitted over long distances.

② Reduces the height of antenna:

Minimum height of the antenna is,

$$h = \lambda/4 = \frac{c}{4f} \quad \left(\because \lambda = \frac{c}{f}\right)$$

[$\lambda \rightarrow$ Wavelength (m), $c \rightarrow$ Velocity of light (3×10^8 m/s), $f \rightarrow$ Frequency Hz]

If $f = 1KHz$, $h = \frac{3\times10^8}{4\times1\times10^3} = 75,000\ m$

(Impractical)

If $f = 1MHz$, $h = \frac{3\times10^8}{4\times1\times10^6} = 75m$ (Practical)

③ Avoid mixing of signals:

Modulation avoids mixing of signals (by using different carrier frequencies for different signals)

④ Allows multiplexing of signals:

Modulation allows the transmission of two or more signals simultaneously over the same channel (multiplexing)

⑤ Improves the quality of reception & Reduces noise:

Modulation reduces the effect of noise & thus improves the quality of reception

⑥ Allows adjustments in bandwidth

Modulation allows to vary the bandwidth of the signal (modulated signal)

⑦ Wireless Communication:

Modulation avoids the use of wires (sometimes). ie Signal can be radiated into free space

* Modulation:

The process of changing one of the characteristics (Eg. Amplitude, frequency or Phase) of a carrier signal (High frequency signal) with respect to the instantaneous values of the message signal (Low frequency signal) is called modulation.

Note: ① The message signal is given by.

$$m(t) = V_m \sin \omega_m t$$

Where V_M → Peak @ maximum Amplitude of message signal

ω_m → Angular frequency of the message signal.

② The carrier signal is given by,

$$C(t) = V_c \sin(\omega_c t + \phi)$$

Where, V_c → Peak @ maximum Amplitude of carrier signal.

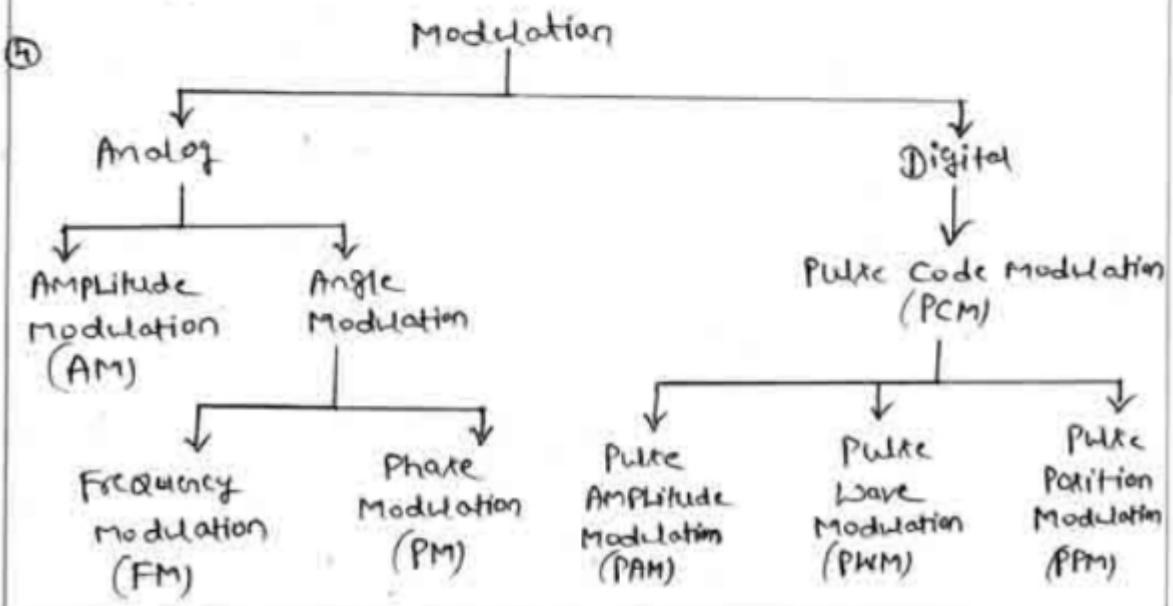
ω_c → Angular frequency of the carrier signal

ϕ → Phase angle of the carrier signal with respect to some reference.

③ Demodulation @ detection

The process of recovering (extracting) the information signal (message signal) from the modulated signal is called demodulation @ detection

④



Types of modulation:

There are three basic types of modulation.

① Amplitude Modulation
② Frequency Modulation] → Angle Modulation
③ Phase Modulation.

① Amplitude Modulation (AM):

The process of changing the amplitude of carrier wave with respect to the instantaneous values of the message signal is called Amplitude modulation (AM)

→ Here the frequency & phase of the carrier wave is kept constant

→ During the positive half-cycle of the message signal, the amplitude of the carrier wave is increased

→ During the negative half-cycle of the message signal, the amplitude of the carrier wave is decreased.

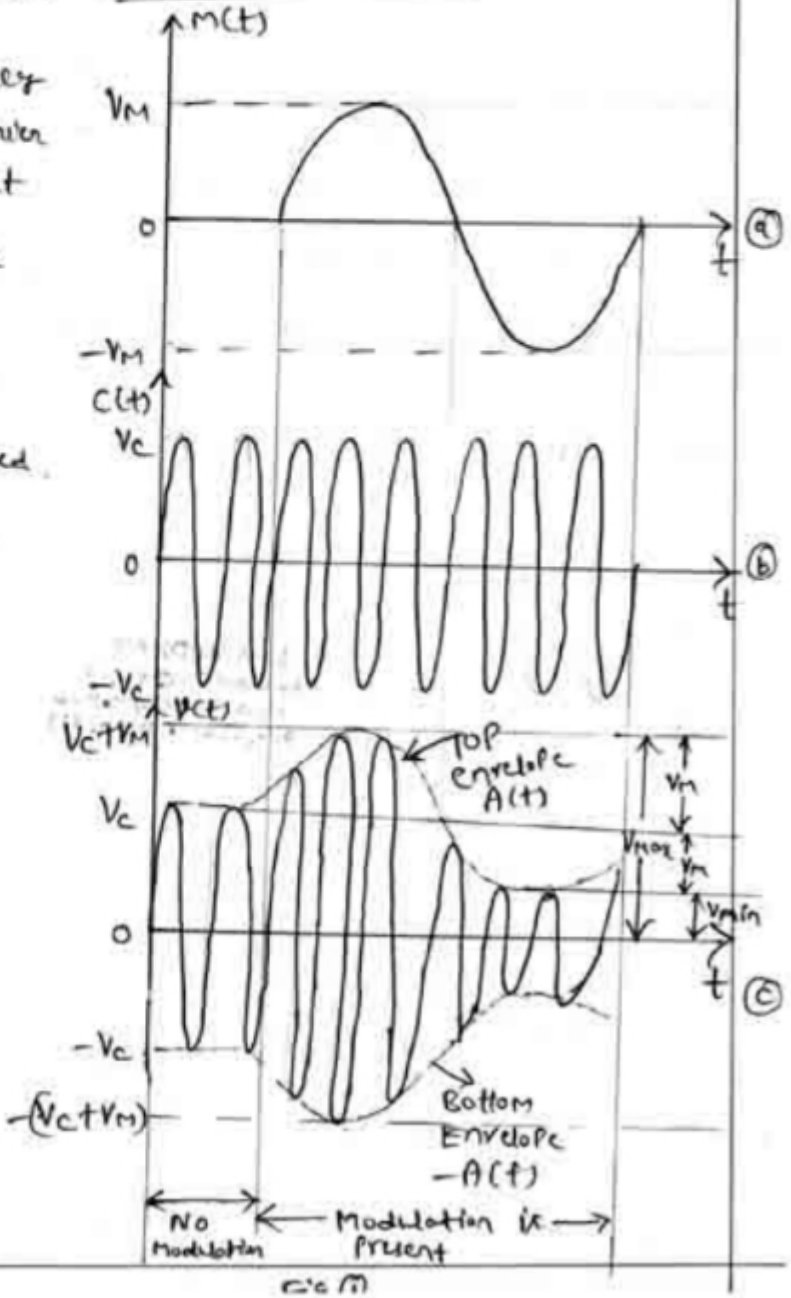


Fig (1)

* AM Wave Equation @ Instantaneous Voltage of AM Wave

Let the message signal is given by,

$$m(t) = V_m \sin \omega_m t \quad -(1)$$

$V_m \rightarrow$ Peak amplitude of message signal

$\omega_m \rightarrow$ Angular frequency of message signal

& the carrier signal is,

$$c(t) = V_c \sin \omega_c t \quad -(2)$$

$V_c \rightarrow$ Peak amplitude of carrier signal

$\omega_c \rightarrow$ Angular frequency of carrier signal.

(Instantaneous amplitude)
The Amplitude of the AM wave (modulated carrier) is,

$$A(t) = V_c + K_a m(t)$$

$$= V_c + K_a V_m \sin \omega_m t \quad [\text{using } (1)] \quad -(3)$$

($K_a \rightarrow$ Amplitude sensitivity of the modulator)

The AM wave @ Instantaneous Voltage of AM wave is,

$$v(t) = A(t) \sin \omega_c t \quad -(4)$$

Using (3) in (4), we get

$$v(t) = (V_c + V_m \sin \omega_m t) \sin \omega_c t \quad (\text{Let } K_a = 1)$$

$$\Rightarrow v(t) = V_c \sin \omega_c t + V_m \sin \omega_c t \sin \omega_m t$$

$$\Rightarrow \boxed{v(t) = V_c \sin \omega_c t + \frac{V_m}{2} \cos(\omega_c - \omega_m)t - \frac{V_m}{2} \cos(\omega_c + \omega_m)t} \quad -(5)$$

$$\because \sin A \sin B = \frac{1}{2}[\cos(A-B) - \cos(A+B)]$$

Let $m = \frac{V_m}{V_c} \Rightarrow V_m = mV_c \quad -(6)$

Using (6) in (5), we get

$$\boxed{v(t) = \underset{\text{carrier}}{V_c \sin \omega_c t} + \underset{\text{@ Difference frequency Lower side band (LSB)}}{\frac{mV_c}{2} \cos(\omega_c - \omega_m)t} - \underset{\text{Sum Frequency @ Upper side band (USB)}}{\frac{mV_c}{2} \cos(\omega_c + \omega_m)t} \quad -(6)}$$

Eqn ⑤ & ⑥ are AM wave & Instantaneous Voltage of AM wave

Note: ① From Eqn ⑤ & ⑥, the AM wave consists of

ⓐ A carrier at frequency (f_c) & with amplitude V_c

ⓑ LSB at frequency $(f_c - f_m)$ & with amplitude $\frac{mV_c}{2}$ & $\frac{V_m}{2}$

ⓒ USB at frequency $(f_c + f_m)$ & with amplitude $\frac{mV_c}{2}$ & $\frac{V_m}{2}$

② Modulation Factor & modulation index (m) (Depth of Modulation)

It is defined as the amount by which the carrier amplitude gets modified by the modulating signal.

It is ratio of the peak amplitude of message (V_m) signal to the peak amplitude of carrier signal (V_c)

ie $$m = \frac{V_m}{V_c} \quad -(7)$$ & $$m = \frac{V_m}{V_c} \times 100\%$$

③ Frequency Spectrum of AM wave & Spectrum:

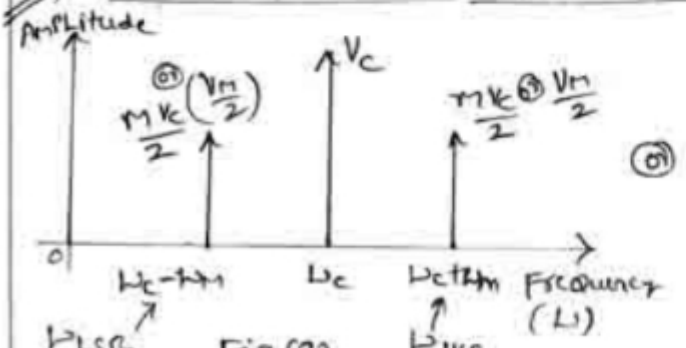


Fig (2)

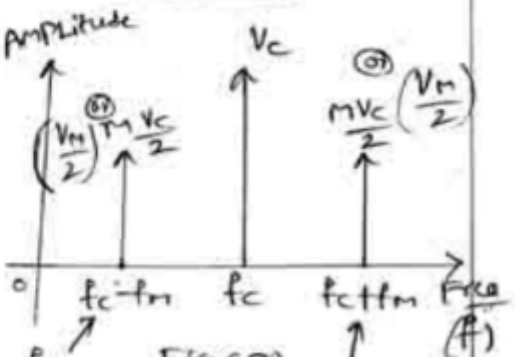


Fig (3)

④ Bandwidth: It is range of frequencies between Lower side & Upper side frequencies.

(f_{LSB}) (f_{USB})

$f_{USB} - f_{LSB}$ $\omega_{USB} - \omega_{LSB}$

ie $BW = (f_c + f_m) - (f_c - f_m)$ or $(\omega_c + \omega_m) - (\omega_c - \omega_m)$

$$\boxed{BW = 2f_m \text{ (Hz)}} \quad -(8) \qquad \boxed{BW = 2\omega_m \text{ (rad/s)}} \quad -(9)$$

(5) Effect of Modulation index on AM

Case(i): $(m > 1)$

→ The carrier is said to be over damped

→ AM wave is distorted (CLIPPED off)

Case(ii): $(m = 1)$.

→ The carrier is said to be Critically damped

Case(iii): $(m < 1)$

→ The carrier is said to be under-damped

∴ Modulation index should not exceed 1

∴ $\boxed{m \leq 1}$

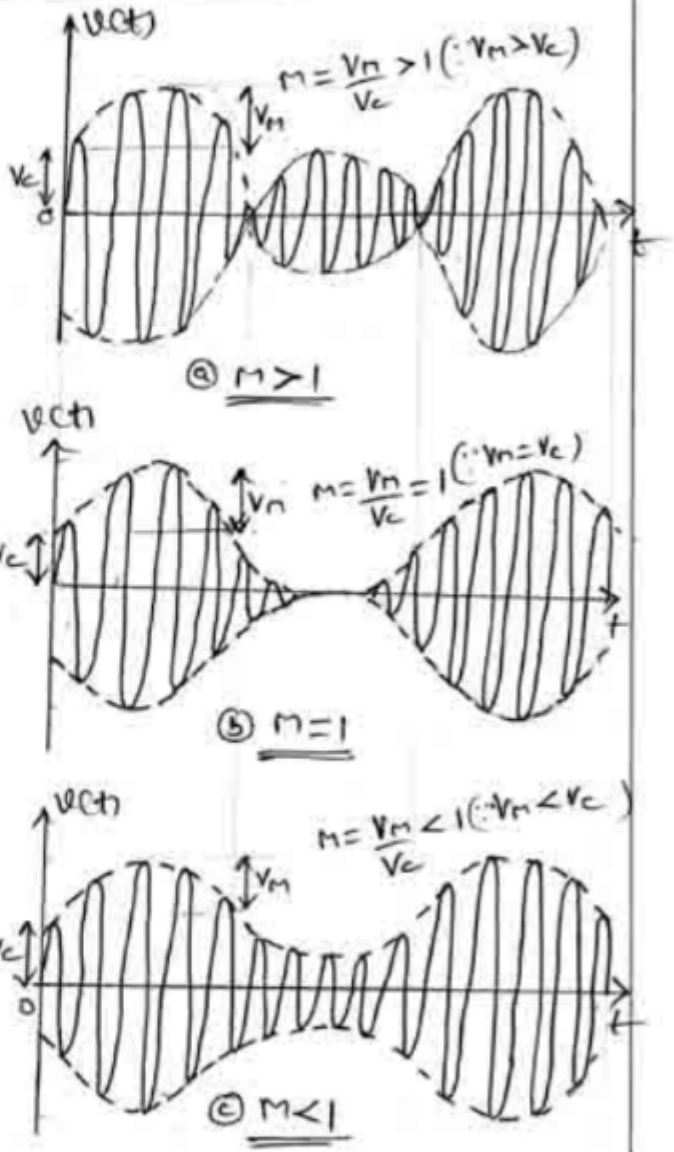


Fig (4): Effect of Modulation index (m) on AM

(6) Expression for modulation index of AM (m in terms of V_{max} & V_{min})

From fig (1)(c), we can write

$$V_{max} = 2V_m + V_{min}$$

$$\Rightarrow 2V_m = V_{max} - V_{min}$$

$$\Rightarrow V_m = \frac{V_{max} - V_{min}}{2} \quad -(10)$$

&

$$V_c = V_m + V_{min} \quad -(11)$$

Using (10) in (11), we get

$$V_c = \frac{V_{max} - V_{min}}{2} + V_{min}$$

$$V_c = \frac{V_{max} + V_{min}}{2} \quad -(12)$$

Let $m = \frac{V_m}{V_c} \quad -(13)$

Using (10) & (12) in (13), we get

$$m = \frac{\frac{V_{max} - V_{min}}{2}}{\frac{V_{max} + V_{min}}{2}}$$

$$m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}} \quad -(14)$$

(or)

$$m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}} \times 100\% \quad -(15)$$

---

* Expression for total average power of a AM wave

(8) Spectrum power in AM wave

AM wave is given by,

$$v(t) = \underbrace{V_c \sin\omega_c t}_{\text{Unmodulated Carrier}} + \underbrace{\frac{mV_c}{2}\cos(\omega_c - \omega_m)t}_{\text{Lower Sideband}} - \underbrace{\frac{mV_c}{2}\cos(\omega_c + \omega_m)t}_{\text{Upper Sideband}}$$

The total power P_t is given by,

$$P_t(\text{total}) = P_{car}(\text{carrier}) + P_{LSB}(\text{LSB}) + P_{USB}(\text{USB}) \quad -(16)$$

$$\Rightarrow P_t = \frac{V_{car}^2}{R} + \frac{V_{LSB}^2}{R} + \frac{V_{USB}^2}{R} \quad -(17) \quad \left[\because \text{Power } P = \frac{V^2}{R}\right]$$

Where, V_{car} → RMS Value of carrier @ Unmodulated carrier

V_{LSB} → RMS Value of Lower sideband

V_{USB} → RMS Value of Upper sideband.

R → Resistance

$\therefore V_{car} = \frac{V_c}{\sqrt{2}}$ — (18), $V_{LSB} = \frac{\frac{mV_c}{2}}{\sqrt{2}}$ — (19), $V_{USB} = -\frac{\frac{mV_c}{2}}{\sqrt{2}}$ — (20) $\left(\because V_{rms} = \frac{V_{max}}{\sqrt{2}}\right)$

Using (18), (19) & (20) in (17) we get.

$$P_t = \frac{(V_c/\sqrt{2})^2}{R} + \frac{\left(\frac{mV_c}{2}/\sqrt{2}\right)^2}{R} + \frac{\left(\frac{mV_c}{2}/\sqrt{2}\right)^2}{R}$$

$$\Rightarrow P_t = \frac{V_c^2}{2R} + \frac{m^2}{4}\frac{V_c^2}{2R} + \frac{m^2}{4}\frac{V_c^2}{2R}$$

$$P_t = \frac{V_c^2}{2R}\left(1 + \frac{m^2}{4} + \frac{m^2}{4}\right)$$

$$\boxed{P_t = \frac{V_c^2}{2R}\left(1 + \frac{m^2}{2}\right)} \text{ (or) } \boxed{P_t = P_{car}\left(1 + \frac{m^2}{2}\right)}$$

— (21) — (or) — (22)

where $P_{car} = \frac{V_c^2}{2R}$

Eqn (21) & (22) is the expression for total power in AM wave

Note:

(1) From (21) & (22) we can say, (a) Total Power in AM wave is more than carrier power

(b) Total power depends on the modulation index m.

(2) Maximum power in an AM wave

From eqn (22), $P_t = P_{car}\left(1 + \frac{m^2}{2}\right)$

Maximum value of m is 1

$\therefore P_t = P_{car}\left(1+\frac{1}{2}\right)$

$P_t = 150\%$ of P_{car} $\boxed{P_t = 1.5 P_{car}}$ // — (23) or $\boxed{P_{car} = 66.66\% P_t}$

Thus the maximum power in AM wave is 1.5 P_c or 150% of the carrier power P_{car}

(3) Modulation index (m) interms of carrier power (P_{car}) & total power of AM wave (P_t)

From eqn (22), $P_t = P_{car}\left(1+\frac{m^2}{2}\right)$

$$\Rightarrow \frac{P_t}{P_{car}} = 1+\frac{m^2}{2}$$

$$\Rightarrow \frac{m^2}{2} = \frac{P_t}{P_{car}} - 1$$

$$\Rightarrow m^2 = 2\left(\frac{P_t}{P_{car}} - 1\right)$$

$$\Rightarrow \boxed{m = \sqrt{2\left(\frac{P_t}{P_{car}} - 1\right)}} \quad — (24)$$ //

(4) Current relation in AM wave (Voltage relation)

From eqn (22), $P_t = P_{car}\left(1+\frac{m^2}{2}\right)$

[$\because$ Power, $P = VI = I^2R = V^2/R$]

$$\Rightarrow I_t^2 R = I_{car}^2 R\left(1+\frac{m^2}{2}\right)$$

$$\Rightarrow \boxed{I_t = I_{car}\sqrt{1+\frac{m^2}{2}}} \text{ (NOT)} \quad — (25) \qquad \boxed{I_{car} = \frac{I_t}{\sqrt{1+\frac{m^2}{2}}}} \text{ (A)} \quad — (26)$$

(or)

$$\boxed{m = \sqrt{2\left(\frac{I_t^2}{I_{car}^2} - 1\right)}} \quad — (27)$$ //

$\because$ WKT $\boxed{m = \sqrt{2\left(\frac{V_t^2}{V_{car}^2} - 1\right)}}$

⑤ Modulation index & total power when a carrier is amplitude modulated by several sine waves :

Let V_1, V_2, V_3 — etc be amplitudes of sine waves, Then the total modulating voltage V_t is,

$$V_t = \sqrt{V_1^2 + V_2^2 + V_3^2 + \cdots}$$

$$\Rightarrow \frac{V_t}{V_c} = \frac{\sqrt{V_1^2 + V_2^2 + V_3^2 + \cdots}}{V_c}$$

$$\Rightarrow \frac{V_t}{V_c} = \sqrt{\left(\frac{V_1}{V_c}\right)^2 + \left(\frac{V_2}{V_c}\right)^2 + \left(\frac{V_3}{V_c}\right)^2 + \cdots}$$

$$\boxed{m_t = \sqrt{m_1^2 + m_2^2 + m_3^2 + \cdots}} \quad \text{— (28)} \qquad (m_t \leq 1)$$

Where, $m_t = \frac{V_t}{V_c}$ → total modulation index

$m_1 = \frac{V_1}{V_c}$, $m_2 = \frac{V_2}{V_c}$ → Individual modulation indices

From eqn (28), the total modulation index is the square root of the sum of the squares of the individual modulation indices.

The total power in the AM wave is,

$$\boxed{P_t = P_{car}\left(1 + \frac{m_t^2}{2}\right)} \quad \text{— (29)}$$

⑥ Transmission efficiency of AM wave :

The ratio of the power carried by the sideband (P_{SB}) (or) power that contains information) to the total power (P_t) is called transmission efficiency (or) Efficiency (η)

Transmission efficiency is,

$$\eta = \frac{P_{SB}}{P_t} \quad \text{— (30)}$$

$$= \frac{P_{LSB} + P_{USB}}{P_t}$$

$$= \frac{\frac{m^2}{4}\frac{V_c^2}{2R} + \frac{m^2}{4}\frac{V_c^2}{2R}}{\frac{V_c^2}{2R}\left(1+\frac{m^2}{2}\right)}$$

$$\frac{\frac{V_c^2}{2R}\left(\frac{m^2}{4}+\frac{m^2}{4}\right)}{\frac{V_c^2}{2R}\left(1+\frac{m^2}{2}\right)}$$

$$\eta = \frac{\frac{m^2}{2}}{1+\frac{m^2}{2}}$$

$$\eta = \frac{m^2}{2+m^2} \quad \text{— (31)} \qquad \text{(or)} \qquad \%\eta = \frac{m^2}{2+m^2} \times 100\% \quad \text{— (32)}$$

$$\because P_{LSB} = \frac{V_{LSB}^2}{R} = \frac{\left(\frac{mV_c}{2}/\sqrt{2}\right)^2}{R}$$

$$P_{USB} = \frac{V_{USB}^2}{R} = \frac{\left(\frac{mV_c}{2}/\sqrt{2}\right)^2}{R}$$

$$P_t = \frac{V_c^2}{2R}\left(1+\frac{m^2}{2}\right)$$

From (31) & (32), it is clear that the transmission efficiency increases with modulation index.

(i) When $m=0$, $\eta = \frac{0}{2+0} = 0$

(ii) When $m=0.5$, $\eta = \frac{0.5}{2+0.5} = 11.1\%$

(iii) When $m=1$, $\eta = \frac{1}{1+2} = 33.33\%$ (max value of m is 1)

∴ Higher the modulation index, higher is the transmission efficiency & maximum efficiency in AM is 33.33%.

* AM detection (demodulation) or (Envelope detector):

→ The process of recovering the message signal (audio signal) from the modulated signal is known as demodulation or detection (ie demodulation is the reverse of the modulation)

→ Fig ⑤ shows the envelope detector. It consists of a diode followed by a RC circuit.

→ Demodulation of AM involves two steps

① Diode eliminates the bottom envelope

② RC circuit (LPF) removes the high frequency carrier

→ The signal 'v(t)' is passed through a diode to cut off the bottom half (Lower half)

→ During positive half-cycle of the input, the diode is forward biased & the capacitor 'C' charges to peak value of the input signal. When the input signal falls below the peak value, the diode becomes reverse-biased & the capacitor 'C' discharges through the load resistor 'R'. The discharging process continues until the

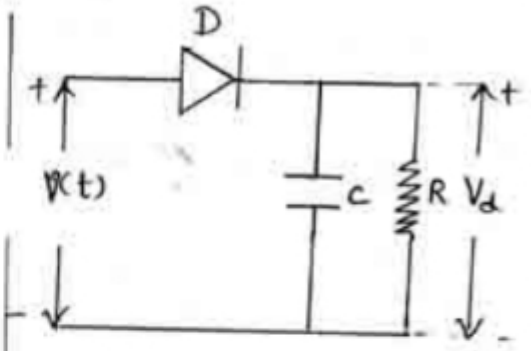


Fig ⑤: Envelope detector

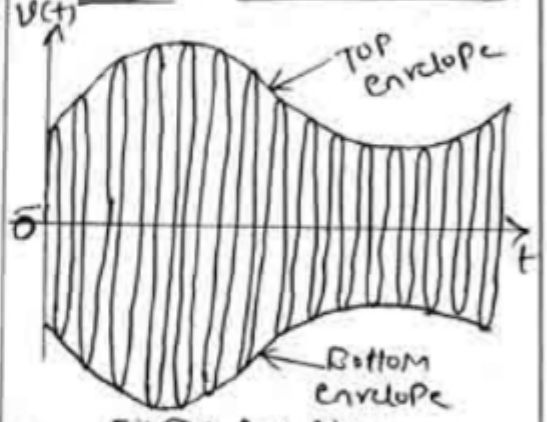


Fig ⑥: AM signal

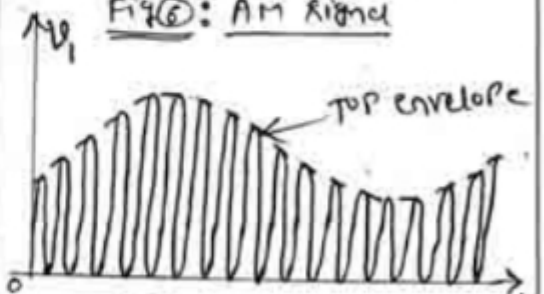


Fig ⑦: Rectified output

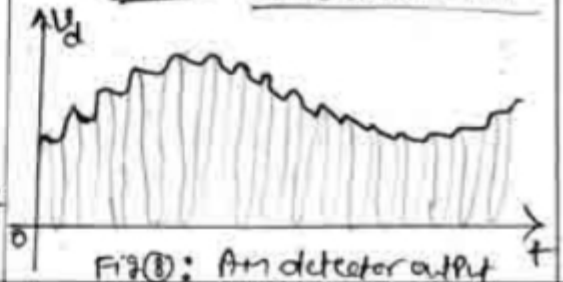


Fig ⑧: AM detector o/p

next +ve positive half cycle.

→ When the input signal becomes greater than the voltage across the capacitor, the diode conducts again & the process is repeated. (O/P V/g 'Vd' follows the modulated wave envelope)

→ The time constant (RC) must satisfy the following conditions

$RC >> T_c$ & $RC << T_m$ $\left(\because T = \frac{1}{f} = \frac{2\pi}{\omega}, \ \omega = 2\pi f\right)$

$\Rightarrow RC >> \frac{2\pi}{\omega_c}$ — (33) $\Rightarrow RC << \frac{2\pi}{\omega_m}$ — (34)

From (33) & (34),

$$\boxed{\frac{2\pi}{\omega_c} << RC << \frac{2\pi}{\omega_m}} \quad — (35)$$

→ The detected envelope is,

$$V_d = V_c + MV_c \sin \omega_m t$$

Where, V_c → dc component can be easily removed by a simple RC LPF

$$\therefore \boxed{V_d = V_m \sin \omega_m t} \rightarrow \text{Message signal} \quad \left[\because M = \frac{V_m}{V_c} \Rightarrow MV_c = V_m\right]$$

Note: ① Fig (5) is equivalent to fig (9) shown below,

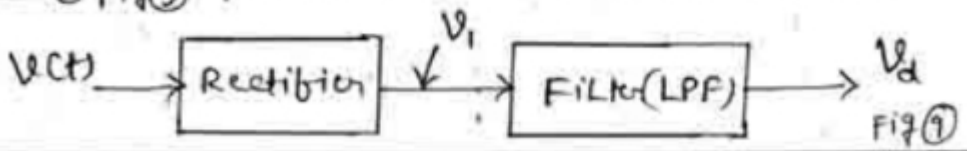


Fig (9)

3) Frequency Modulation (FM):

The process of changing the frequency of carrier wave with respect to the instantaneous values of the message signal is called frequency modulation (FM)

→ Here the amplitude & phase of the carrier wave is kept constant.

→ When the message signal voltage is zero as at A, C, & E, the carrier frequency is unchanged (remains at frequency f_c)

→ When the message signal approaches its positive peak as at B, the carrier frequency is increased to maximum as shown by the closely spaced cycles. (High frequency)

→ When the message signal approaches its negative peak as at D, the carrier frequency is reduced to minimum as shown by the widely spaced cycles. (Low frequency)

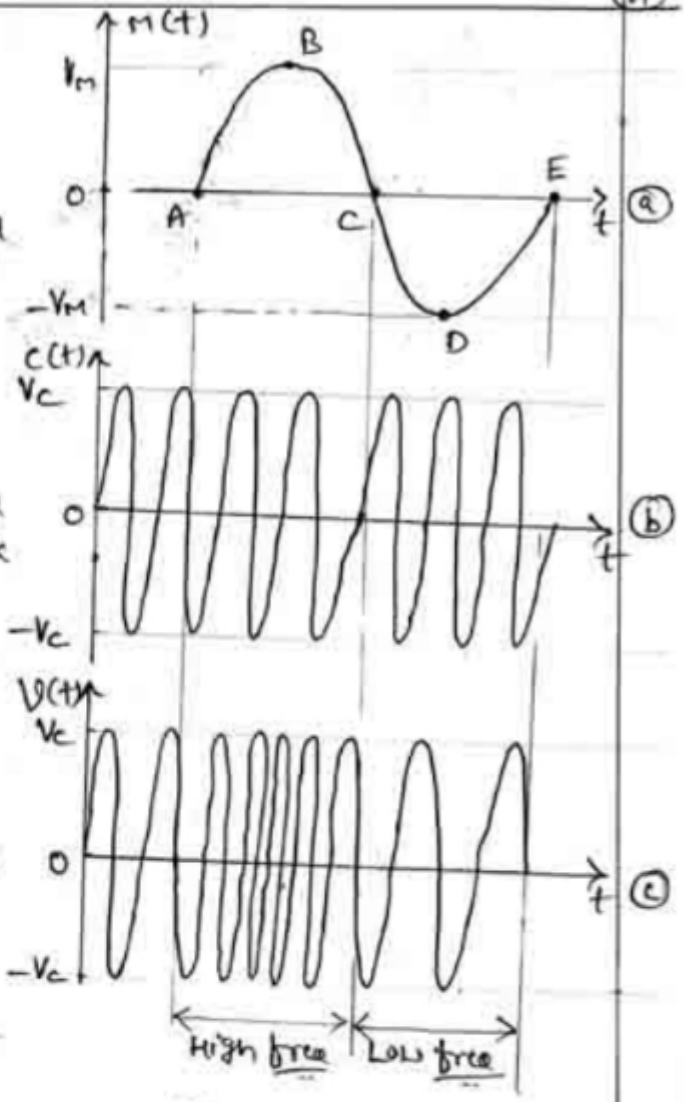


Fig ①

FM wave equation @ Instantaneous Voltage of FM wave :

Let the instantaneous frequency of the FM wave,

$$f_i = f_c(1 + K V_m \cos\omega t) \quad \text{— ①}$$

Where, f_c → carrier frequency

K → Constant of proportionality

Let the angular frequency of the FM wave is,

$$\omega_i = \frac{d\theta_i}{dt}$$

$$\Rightarrow \theta_i = \int_0^t \omega_i \, dt \quad -(4)$$

$$\Rightarrow \theta_i = \int_0^t \omega_c (1 + K V_m \cos 2\pi f_m t) \, dt$$

$$\Rightarrow \theta_i = \int_0^t \omega_c \, dt + \int_0^t \omega_c K V_m \cos(2\pi f_m t) \, dt$$

$$\Rightarrow \theta_i = \omega_c t + \frac{\omega_c K V_m \sin(2\pi f_m t)}{2\pi f_m}$$

$$\Rightarrow \theta_i = \omega_c t + \frac{2\pi f_c K V_m \sin(2\pi f_m t)}{2\pi f_m}$$

$$\Rightarrow \theta_i = \omega_c t + \frac{K_f V_m \sin(2\pi f_m t)}{f_m}$$

Where $K_f = K f_c$
↓
Frequency sensitivity of FM or Deviation constant

$$\Rightarrow \theta_i = \omega_c t + \frac{\Delta f}{f_m} \sin(2\pi f_m t) \quad -(5)$$

$$\Rightarrow \theta_i = \omega_c t + \beta \sin(2\pi f_m t) \quad -(6)$$

Where,
$\Delta f = K_f V_m$
↓
Frequency deviation

The FM wave is,

$$V(t) = V_c \cos \theta_i \quad -(7)$$

Using (6) in (7), we get

$$V(t) = V_c \cos[\omega_c t + \beta \sin(2\pi f_m t)] \quad -(8)$$

$\beta = \frac{\Delta f}{f_m}$
↓
Modulation index
or
Modulation factor
or
Phase deviation of FM signal

or

$$V(t) = V_c \cos[(2\pi f_c t) + \beta \sin(2\pi f_m t)] \quad -(9)$$

Let the message signal is,

$$m(t) = V_m \cos \omega_m t \quad -(2)$$

& the carrier signal is,

$$c(t) = V_c \cos \omega_c t \quad -(3)$$

$\omega_m = 2\pi f_m$ &
$\omega_c = 2\pi f_c$

$\because$ From (1),

$f_i = f_c (1 + K V_m \cos \omega_m t)$

$\Rightarrow 2\pi f_i = 2\pi f_c (1 + K V_m \cos \omega_m t)$

$\Rightarrow \omega_i = \omega_c (1 + K V_m \cos \omega_m t)$

where $\omega_m = 2\pi f_m$

Eqn ⑧ & ⑨ are the expression for FM wave

Note: ① Modulation index for (FM): (β)

Modulation index is defined as the ratio of the frequency deviation to the modulating frequency.

ie $\beta = \frac{\Delta f}{f_m}$ (or) $\frac{\Delta \omega}{\omega_m}$ —⑩

β is generally greater than 1 (measured in radians)

② Frequency Spectrum:

FM consists of ⓐ carrier (at f_c)

ⓑ Infinite number of sidebands

Upper sideband frequencies at $f_c + f_s$, $f_c + 2f_s$, ...

Lower sideband frequencies at $f_c - f_s$, $f_c - 2f_s$, ...

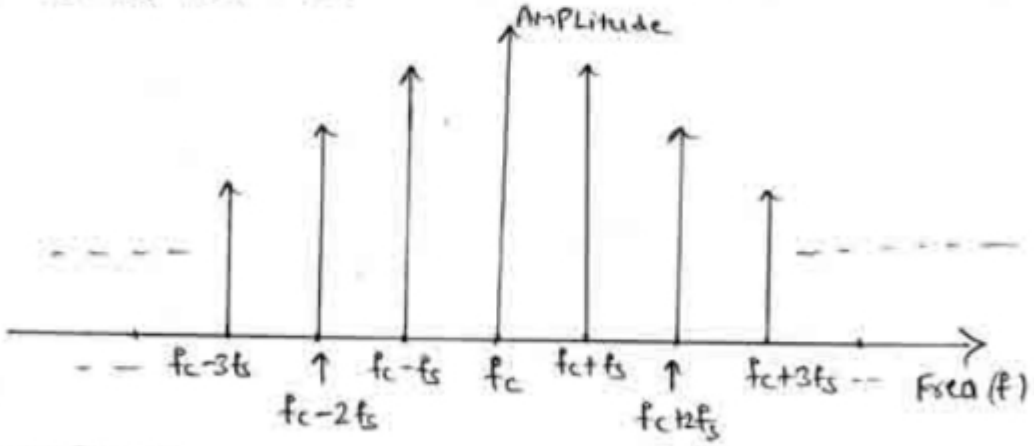


Fig ②: Frequency Spectrum of FM

③ Bandwidth:

From Carson's rule, the BW of FM is,

$$BW = 2(\Delta f + f_m) \text{ (or) } 2\Delta f\left(1 + \frac{1}{\beta}\right) \quad \text{—⑪}$$

(or)

$$BW = 2\beta f_m + 2f_m \text{ (or) } 2f_m(\beta + 1)$$

- If $\Delta f > f_m$, it is Wideband FM
- If $\Delta f < f_m$, it is narrowband FM.

④ Total power in FM wave (P_t)

$$P_t = \frac{V_c^2}{2} \sum_{n=-\infty}^{\infty} J_n^2(\beta) \quad -(12)$$

where,
$J_n(\beta)$ → Bessel function.

⑤ Frequency deviation

Consider eqn(1),

$$f_i = f_c(1 + K V_m \cos \omega_m t)$$

$$\Rightarrow f_i = f_c + K f_c V_m \cos \omega_m t$$

Maximum value of f_i occurs when $\cos \omega_m t = \pm 1$

$$\therefore f_i = f_c \pm K f V_m \quad -(13)$$

Comparing (13) with $f_i = f_c \pm \Delta f$ $-(14)$

$$\boxed{\Delta f = K f_c V_m}$$ → Frequency deviation (or) Maximum frequency deviation.

③ Phase Modulation (PM):

The process of changing the phase of carrier wave with respect to the instantaneous values of the message signal is called Phase modulation (PM)

→ Here the amplitude & frequency of the carrier wave is kept constant.

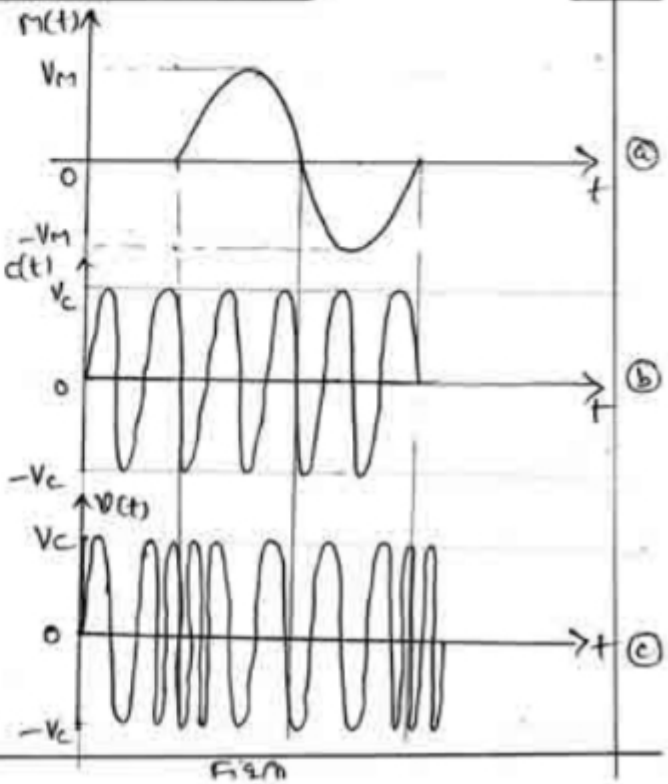


Fig n

* PM Wave Equation @ Instantaneous Voltage of PM Wave

Let the message signal is,

$$m(t) = V_m \cos \omega_m t \quad -①$$

[Angular freq of m(t) is, $\omega_m = 2\pi f_m$]

& the carrier signal is,

$$c(t) = V_c \cos \omega_c t \quad -②$$

[Angular freq of c(t) is, $\omega_c = 2\pi f_c$]

Let the instantaneous phase of the modulated carrier (PM wave) is,

$$\theta_i = \omega_c t + K_p m(t) \quad -④$$

$$\Rightarrow \theta_i = \omega_c t + K_p V_m \cos \omega_m t$$

$$\Rightarrow \boxed{\theta_i = \omega_c t + m_p \cos \omega_m t} \quad -③$$

[K_p → Frequency deviation (rad/V) @ Phase Sensitivity of PM @ Constant of Proportionality for PM]

[Where, $m_p = K_p V_m$ ↓ Modulation index]

The PM wave is,

$$v(t) = V_c \cos \theta_i \quad -④$$

Using ③ in ④, we get

$$\boxed{v(t) = V_c \cos(\omega_c t + m_p \cos \omega_m t)} \quad -⑤$$

@

$$\boxed{v(t) = V_c \cos(2\pi f_c t + m_p \cos 2\pi f_m t)} \quad -⑥$$

Eqn ⑤ & ⑥ are the expression for PM wave.

Note: ① Now differentiating eqn ④ we get (w.r.t t)

$$\omega_i = \omega_c + K_p \frac{d}{dt} m(t)$$

[$\because \frac{d\theta_i}{dt} = \omega_i$, $\frac{d(t)}{dt} = 1$]

$$\Rightarrow 2\pi f_i = 2\pi f_c + K_p \frac{d}{dt} m(t)$$

$$\Rightarrow f_i = f_c + \frac{K_p}{2\pi} \frac{d}{dt} m(t) \quad -⑦$$

Eqn ⑦ is the instantaneous freq of PM wave

② Band Width

$BW = 2f_m(K_p V_m + 1)$ @ $2f_m(m_p + 1)$

③ The average transmitted power of angle modulated wave (both FM & PM) is,

$$P_{av} = \frac{1}{2} V_c^2$$

$$\left[P_{av} = \frac{V_{con}^2}{R} = \frac{\left(\frac{V_c}{\sqrt{2}}\right)^2}{R} = \frac{V_c^2}{2} \right], \quad R = 1\Omega$$

---

* Advantages of AM (merits):

① Bandwidth required is less (compared to FM & PM)
② Demodulation of AM is much SIMPLER (compared to FM)
③ AM receivers are cheap. ⑤ AM is a linear process
④ Wider coverage area (compared to FM)

* Disadvantages of AM @ Drawbacks @ Demerits:

① Transmission efficiency is poor ($\eta_{max} \leq 33.33\%$)
② Poor audio quality
③ Affected by noise
④ Limited operating range
⑤ Affected by electrical storms & other radio frequency interference

* Advantages of FM

① Better audio Quality (compared to AM)
② Efficiency is high ($\eta \leq 100\%$)
③ More immune to noise (compared to AM)
④ operating range is quite large

⑤ No adjacent channel interference

⑥ Transmitted power is constant & independent of modulation depth ⑦ Signal to noise ratio can be improved

* Disadvantages of FM

① Bandwidth required is much larger (compared to AM)

② Cannot be transmitted over long distances (Area of reception is small)

③ Complex & expensive transmitting & receiving equipments.

④ Jamming of FM signal is easier than for AM.

⑤ Presence of tall buildings ⑥ Land masses may limit the coverage & Quality of FM.

* Comparision between AM & FM

AM	FM
① Amplitude of the carrier changes (Frequency & phase remains constant) (EM wave)	① Frequency of the carrier changes (Amplitude & phase remains constant) (EM wave)
② Modulation index varies from 0 to 1	② Modulation index is much greater than 1
③ More susceptible to noise	③ Less susceptible to noise
④ It has two sidebands	④ It has infinite number of sidebands
⑤ Transmitter & receiver are simple (IF for AM RX = 455 KHz)	⑤ Transmitter & receiver are more complex (IF for FM RX = 10.7 MHz)
⑥ Bandwidth = $2f_m$ (BW is less) ($\simeq$ 10KHz)	⑥ BW = $2(\Delta f + f_m)$ ($\simeq$ 200KHz) (BW is more compared to AM)
⑦ All transferred power is not useful	⑦ All power is useful.
⑧ Poor audio Quality	⑧ Better audio Quality

⑨ More prone to interference	⑨ Less prone to interference
⑩ Transmission efficiency is less ($\leq 33.33\%$)	⑩ Better efficiency ($\leq 100\%$)
⑪ Frequency ranges from 535 KHz to 1705 KHz	⑪ Frequency ranges from 88 MHz to 108 MHz.
⑫ Covers long distance	⑫ Covers small distances
⑬ origin – 1870s (mid)	⑬ origin – 1930's
⑭ Propagation is by ground & sky waves	⑭ Propagation is by space waves
⑮ Cannot handle weaker signals	⑮ Can handle weaker signals
⑯ AM wave is $v(t) = V_c[1 + M\sin\omega_m t]\sin\omega_c t$	⑯ FM wave is $v(t) = V_c \cos[2\pi f_c t + \beta \sin 2\pi f_m t]$
⑰ Zero crossing is equidistant	⑰ Zero crossing is not equidistant.

* Features of PM:

① Zero crossing of PM do not occur at regular intervals of time (For FM also)

② The envelope of PM wave is constant compared to AM (For FM also)

③ Instantaneous value of PM (& also FM) is a non-linear function of the information signal.

④ Phase of the carrier changes (Frequency & amplitude remains constant)

⑤ PM wave is, $v(t) = V_c \cos(2\pi f_c t + M_p \cos 2\pi f_m t)$

⑥ PM is indirect method of producing FM

⑦ Modulation index, $M_p = K_p V_m$

⑧ $BW = 2f_m(M_p + 1)$ (BW is more)

⑨ Average transmitted power, $P_{av} = \frac{1}{2} V_c^2$

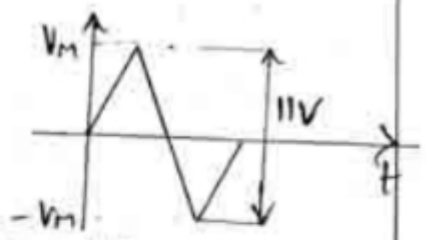
(10) PM is more immune to noise
(11) Less prone to interference
(12) Transmitter & receiver are more complex
(13) Visualization difficult of message waveform

Problems

① A modulating signal consists of a symmetrical triangular wave, which has zero dc component & Peak-to-Peak voltage 11V. It is used to amplitude modulate a carrier of Peak voltage 10V. Calculate the modulation index?

Sol: Peak Amplitude of modulating signal,

$$V_M = \frac{11}{2} = 5.5V$$



From fig, $2V_M = 11V$

Given, $V_c = 10V$

Modulation index, $m = \frac{V_M}{V_c}$

$$= \frac{5.5}{10}$$

$$\boxed{m = 0.55}$$

② A carrier wave of frequency 10MHz & Peak value 10V is amplitude modulated by a 5kHz sine wave of amplitude 6V. Determine the modulation index & amplitude of the side frequencies.

Sol: Given $f_c = 10 \times 10^6 Hz$, $V_c = 10V$,

$f_m = 5 \times 10^3 Hz$, $V_M = 6V$.

Modulation index

$$m = \frac{V_M}{V_c}$$

$$m = \frac{6}{10}$$

$$\boxed{m = 0.6}$$

Amplitude of side frequencies

$$V_{SB} = \frac{mV_c}{2}$$

$$= \frac{0.6 \times 10}{2}$$

$$\boxed{V_{SB} = 3V}$$

③ A broadcast radio transmitter radiates 10KW, when the modulation Percentage is 60. How much of this is carrier power.

Sol: Given $P_t = 10\times10^3$ W, $M = 60\% = 0.6$, $P_{cn} = ?$

We know $P_t = P_{cn}\left(1+\frac{M^2}{2}\right)$

$$\Rightarrow P_{cn} = \frac{P_t}{1+\frac{M^2}{2}}$$

$$= \frac{10\times10^3}{1+0.6^2/2}$$

$$\boxed{P_c = 8.47\text{ KW}}$$ //.

④ A radio transmitter radiates 10KW & carrier power is 8.5KW. Calculate Modulation index.

Sol: Given $P_t = 10$KW, $P_{cn} = 8.5$KW, $M = ?$

We know $P_t = P_{cn}\left(1+\frac{M^2}{2}\right)$

$$\Rightarrow M = \sqrt{2\left(\frac{P_t}{P_{cn}}-1\right)}$$

$$= \sqrt{2\left(\frac{10\times10^3}{8.5\times10^3}-1\right)}$$

$$\boxed{M = 0.59}$$ //.

⑤ A 400W carrier is modulated to a depth of 7.5%. Calculate total power in the modulated wave.

Sol: Given, $P_{cn} = 400$W, $M = 7.5\% = 0.075$, $P_t = ?$

We know $P_t = P_{cn}\left(1+\frac{M^2}{2}\right) = 400\left(1+\frac{0.075^2}{2}\right) = 401.12$ W

(6) The antenna current of an AM transmitter is 8 amps. When only the carrier is sent, but it increases to 8.93A, when the carrier is modulated by a single sine wave. Find Percentage modulation. Determine the antenna current when the percent-modulation changes to 0.8

Sol: Given $I_{car} = 8A$, $I_t = 8.93A$.

$m = ?$

We know $I_t = I_{car}\sqrt{1+\frac{m^2}{2}}$

$\Rightarrow m = \sqrt{2\left[\left(\frac{I_t}{I_{car}}\right)^2 - 1\right]}$

$m = \sqrt{2\left[\left(\frac{8.93}{8}\right)^2 - 1\right]}$

$\boxed{m = 0.7014 \text{ @ } 70.14\%}$

$m = 0.8$, $I_t = ?$

We know

$I_t = I_{car}\sqrt{1+\frac{m^2}{2}}$

$= 8\sqrt{1+\frac{0.8^2}{2}}$

$\boxed{I_t = 9.191A}$ //.

(7) Calculate the modulation index & percentage modulation if instantaneous voltages of modulating signal & carrier are $40\sin 4\pi t$ & $60\sin 2\pi t$ respectively.

Sol: Given $m(t) = 40\sin 4\pi t$ $\quad c(t) = 60\sin 2\pi t$

$\Rightarrow V_m = 40$ $\quad \Rightarrow V_c = 60$

$\therefore$ Modulation index, $m = \frac{V_m}{V_c} = \frac{40}{60} = 0.666$

% Modulation, $m\% = 66.66\%$

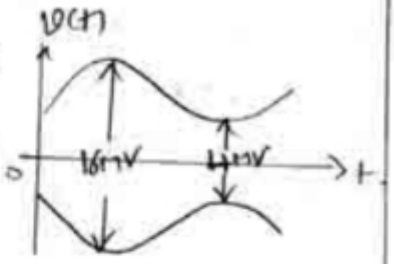
(8) The maximum peak-to-peak voltage of an AM wave is 16mV & the minimum peak-to-peak voltage is 4mV.

Calculate the modulation factor.

Sol:

Given $2V_{max} = 16mV$, $2V_{min} = 4mV$

$\Rightarrow V_{max} = 8mV$, $V_{min} = 2mV$



With modulation factor,

$$m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$$

$$= \frac{8 \times 10^{-3} - 2 \times 10^{-3}}{8 \times 10^{-3} + 2 \times 10^{-3}}$$

$$\boxed{m = 0.6 \text{ @ } 60\%}$$ //

(3) A carrier of 100V & 1200 KHz is modulated by a 50V, 1000Hz sine wave signal. Find the modulation factor.

Sol: Given, $V_c = 100V$, $V_m = 50V$

Modulation factor, $m = \frac{V_m}{V_c} = \frac{50}{100}$

$$\boxed{m = 0.5 \text{ @ } 50\%}$$ //

(4) A 2500KHz carrier is modulated by audio signal with frequency span of 50 - 15000Hz. What are the freq of Lower & Upper sidebands? What bandwidth of RF amplifier is required to handle the output?

Sol: Given $f_c = 2500 \times 10^3$ Hz,

$f_{m_1} = 50$Hz

$LSB_1 = f_c - f_{m_1} = 2499.95$KHz

$USB_1 = f_c + f_{m_1} = 2500.05$KHz

$BW_1 = USB_1 - LSB_1$

$f_{m_2} = 15000$Hz.

$LSB_2 = f_c - f_{m_2} = 2485$KHz

$USB_2 = f_c + f_{m_2} = 2515$KHz

$BW_2 = USB_2 - LSB_2$

$BW_1 = 100\,Hz$ $(2f_{m_1})$ | $BW_2 = 30\,KHz$ $(2f_{m_2})$

Upper side band ranges from 2500.05 KHz – 2515 KHz

Lower side band ranges from 2499.95 KHz – 2485 KHz

Bandwidth ranges from 100 Hz – 30 KHz

(10) An AM wave is given by.

$V = 5(1 + 0.6\cos 6280t)\sin 211\times10^4 t$ Volts

(i) What are the minimum & max amplitudes of the AM wave? (ii) What frequency components are contained in the modulated wave & what is the amplitude of each component?

Sol: Given $V = 5(1 + 0.6\cos 6280t)\sin 211\times10^4 t$ — (1)

Comparing it with standard AM wave.

$$V(t) = V_c(1 + m\cos\omega_m t)\sin\omega_c t \quad — (2)$$

From (1) & (2), we get

$V_c = 5V$ | $m = 0.6$, $\Rightarrow \frac{V_m}{V_c} = 0.6$, $\Rightarrow V_m = 0.6\times5$, $V_m = 3V$ | $\omega_m = 6280$, $2\pi f_m = 6280$, $\Rightarrow f_m = \frac{6280}{2\pi}$, $f_m \simeq 1\,KHz$ | $\omega_c = 211\times10^4$, $2\pi f_c = 211\times10^4$, $\Rightarrow f_c = \frac{211\times10^4}{2\pi}$, $f_c = 335.816\,KHz$

(i) Minimum & max amplitudes of AM wave

$V_{min} = V_c - V_m = 5 - 3 = 2V$

$V_{max} = V_c + V_m = 5 + 3 = 8V$

(iii) Freq components & the amplitude of each component

AM wave will contain three frequency components

① carrier: $f_c = 335.816\ KHz$

② LSB: $f_{LSB} = f_c - f_m = 335.816\ KHz - 1\ KHz = 334.816\ KHz$

③ USB: $f_{USB} = f_c + f_m = 335.816 \times 10^3 + 1 \times 10^3 = 336.816\ KHz$

Amplitudes of three components

① carrier: $V_c = 5V$

② LSB: $V_{LSB} = \frac{mV_c}{2} = \frac{3}{2} = 1.5V$

③ USB: $V_{USB} = \frac{mV_c}{2} = \frac{3}{2} = 1.5V$

(12) A FM voltage wave is given by.

$$e = 12\cos(8\times10^8 t + 5\sin 1250 t)$$

Find (i) carrier frequency (ii) signal frequency (iii) modulation index (iv) maximum frequency deviation (v) power dissipated by the FM wave in 1Ω resistor (vi) BW.

Sol:

Given $e = 12\cos(8\times10^8 t + 5\sin 1250 t)$ — (1)

Comparing with $v(t) = V_c\cos(\omega_c t + \beta\sin\omega_m t)$ — (2)

From (1) & (2), $V_c = 12V$, $\omega_c = 8\times10^8$, $\beta = 5$, $\omega_m = 1250$

(i) f_c $f_c = \frac{\omega_c}{2\pi} = \frac{8\times10^8}{2\pi} = 95.5\ MHz$

(ii) f_m $f_m = \frac{\omega_m}{2\pi} = \frac{1250}{2\pi} = 199\ Hz$

(iii) β $\beta = 5$ (no unit)

(iv) Δf $\Delta f = \beta f_m = 5 \times 199 = 995\ Hz$

(v) P

$$P = \frac{V_{rms}^2}{R} = \frac{(V_c/\sqrt{2})^2}{1\Omega} = 7.2\ W$$

(vi) $BW = 2(\Delta f + f_m) = 2(995 + 199) = 2.388\ KHz$

(13) In FM broadcasting $\delta_{max} = 75KHz$, & modulation frequency 15KHz, what is deviation ratio

Sol: Given $\delta_{max} = \Delta f = 75KHz$, $f_m = 15KHz$

$$\beta = \frac{\Delta f}{f_m} = \frac{75K}{15K} = 5 \quad \text{(Deviation ratio)}$$

(14) For an AM wave, the modulated & minimum amplitudes are 500mV & 300mV respectively, find Modulation index & percentage of modulation

Sol: Given $V_{max} = 500mV$, $V_{min} = 300mV$.

We have, $$m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}} = \frac{500\times10^{-3} - 300\times10^{-3}}{500\times10^{-3} + 300\times10^{-3}}$$

Modulation index → $\boxed{m = 0.25}$ Percentage of modulation = 25%.

(5) In a FM SM, audio frequency is 500Hz, AF voltage is 2V & the frequency deviation is 4.8KHz. Find the modulation index.

Sol: Given $f_m = 500Hz$, $V_m = 2V$, $\Delta f = 4.8\times10^3 Hz$, $\beta = ?$

We have, $$\beta = \frac{\Delta f}{f_m} = \frac{4.8\times10^3}{500} = 9.6$$

(6) What is the antenna height required for AM with carrier frequency $f = 4MHz$? $[\because \lambda = c/f]$

Sol: Given $f(f_c) = 4MHz$,

Height (size) of antenna: $h = \frac{\lambda}{4} = \frac{c}{f\times4} = \frac{3\times10^8}{4\times10^6\times4} = 18.75m$

(17) Find the maximum power efficiency of an AM Modulator.

Sol:

W.K.t carrier power $P_{car} = \frac{V_{car}^2}{R} = \frac{(V_c/\sqrt{2})^2}{R} = \frac{V_c^2}{2R}$ — (1)

(Doesnot contain information)

Power contained in sidebands $P_{SB} = P_{LSB} + P_{USB}$

(Contains information

$$= \frac{V_{LSB}^2}{R} + \frac{V_{USB}^2}{R}$$

$$= \frac{\left(\frac{mV_c}{2}/\sqrt{2}\right)^2}{R} + \frac{\left(\frac{mV_c}{2}/\sqrt{2}\right)^2}{R}$$

$$= \frac{m^2 V_c^2}{4R} \quad — (2)$$

Now,

Power efficiency $\eta_p = \frac{P_{SB}}{P_{car}} = \frac{m^2 V_c^2/4R}{V_c^2/2R} = \frac{m^2}{2}$

maximum value of $m = 1$

∴ Maximum power efficiency $\boxed{(\eta_p)_{max} = \frac{1}{2} = 0.5 \text{ @ } 50\%}$ //

(18) The total power content of an AM signal is 1.5kW. Determine the power being transmitted at the carrier freq & at each of the sidebands when the modulation is 50%

Sol: Given $P_t = 1.5 \times 10^3 W$, $m = 50\% = 0.5$, $P_{car} = ?$,

$P_{USB} = ?$, $P_{LSB} = ?$

W.K.t $P_t = P_{car} + P_{USB} + P_{LSB}$ — (1) (or) $P_{car}\left(1 + \frac{m^2}{2}\right)$ — (2)

$$\Rightarrow P_{Car} = \frac{P_t}{1+\frac{M^2}{2}} = \frac{1.5\times10^3}{1+\frac{0.5^2}{2}} = 1.333\ KW$$

Now From ①,

$$P_{USB} + P_{LSB} = P_t - P_{Car}$$
$$= 1.5\times10^2 - 1.333\times10^3$$
$$= 167\ W$$

$$\Rightarrow P_{USB} = P_{LSB} = \frac{167}{2} = 83.5\ W \quad [\because P_{USB} = P_{LSB}]$$

⑩ An AM wave has a Power Content of 1000W at its Carrier frequency. Determine the Power of each sideband for 70% Modulation.

Sol: Given $P_{Car} = 1000W$, $M = 70\% = 0.7$, $P_{LSB} = P_{USB} = ?$

We know $P_{LSB} = P_{USB} = P_{Car}\frac{M^2}{4} = \frac{1000\times0.7^2}{4} = 122.5W$

⑪ Determine modulation factor of signal if each of the sidebands contains 100W. Given total Power of an AM wave = 800W.

Sol: Given $M = ?$, $P_{LSB} = P_{USB} = 100W$, $P_t = 800W$

We know $P_t = P_{Car} + P_{USB} + P_{LSB}$

$$\Rightarrow P_{Car} = P_t - P_{USB} - P_{LSB} = 800 - 100 - 100$$

$$\boxed{P_{Car} = 600W}$$

Also we have $P_t = P_{Car}\left(1+\frac{M^2}{2}\right)$

$$\Rightarrow M = \sqrt{2\left(\frac{P_t}{P_{Car}} - 1\right)} = \sqrt{2\left(\frac{800}{600} - 1\right)} = 0.816$$

81.6%

1) A Sinusoidal carrier voltage of amplitude 150V is amplitude modulated by a signal of freq 1KHz resulting in maximum modulated carrier of 220V. Calculate modulation factor

Sol: Given $V_c = 150V$, $f_m = 1 \times 10^3 Hz$, $V_{max} = 220V$

$m = ?$

We have,

$$m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$$

$$= \frac{220 - 80}{220 + 80} \quad \left[\because V_{min} = 2V_c - V_{max},\ V_{min} = 80V\right]$$

$$m = 0.466 \text{ @ } 46.6\%$$

(or) We have

$$m = \frac{V_m}{V_c} \quad \left[V_m = V_{max} - V_c,\ V_m = 220 - 150,\ V_m = 70\right]$$

$$= \frac{70}{150}$$

$$m = 0.466 \text{ @ } 46.6\%$$

2) An AM transmitter radiates 10KW with the carrier unmodulated & 11KW when the carrier is sinusoidally modulated. Calculate the modulation index. If another sinewave with modulation index 50% is transmitted simultaneously, determine total power.

Sol: Given $P_{car} = 10KW$, $P_t = 11KW$, $m_1 = ?$,

$m_2 = 50\% \text{ @ } 0.5$, $P_{tot} = ?$

We know $P_t = P_{car}\left(1 + \frac{m_1^2}{2}\right)$

$$\Rightarrow m_1 = \sqrt{2\left(\frac{P_t}{P_{car}} - 1\right)} = \sqrt{2\left(\frac{11 \times 10^3}{10 \times 10^3} - 1\right)} = 0.44$$

We know $m = \sqrt{m_1^2 + m_2^2} = \sqrt{0.44^2 + 0.5^2} = 0.66$ (Total modulation index)

Total Power, $P_{total} = P_{car}(1 + m^2/2) = 10 \times 10^3\left(1 + \frac{0.66^2}{2}\right) = 12.178KW$

(23) The antenna current of an AM transmitter, modulated to 50% by a sine wave is 10A. It increases to 11A as a result of simultaneous modulation by another sine wave. What is the modulation index of second wave?

Sol: Given $m_1 = 50\% = 0.5$, $I_{t_1} = 10A$. $I_t = 11A$ (Total), $m_2 = ?$

We know $I_{cn} = \frac{I_{t_1}}{\sqrt{1+\frac{m_1^2}{2}}} = \frac{10}{\sqrt{1+\frac{0.5^2}{2}}} = 9.428A$

Now $I_t = I_{cn}\sqrt{1+\frac{m^2}{2}}$ (Total)

$\Rightarrow m = \sqrt{2\left[\left(\frac{I_t}{I_{cn}}\right)^2 - 1\right]} = \sqrt{2\left[\left(\frac{11}{9.428}\right)^2 - 1\right]} = 0.85$

We know $m^2 = \sqrt{m_1^2 + m_2^2}$

$\Rightarrow m_2^2 = \sqrt{m^2 - m_1^2} = \sqrt{0.85^2 - 0.5^2} = 0.68$

(4) An audio signal is $15\sin(2\pi 2000t)$ Amplitude modulates a carrier signal $60\sin(2\pi 100{,}000t)$. Determine (i) Modulation factor (ii) Frequency of signal & carrier & (iii) Frequency components of modulated wave (iv) Plot the spectrum

Sol: Given $m(t) = 15\sin(2\pi 2000t)$ comparing with $m(t) = V_m \sin(\omega_m t)$

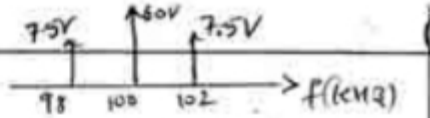
$\Rightarrow \boxed{V_m = 15}$ $\omega_m = 2\pi f_m = 2\pi 2000$ $\Rightarrow \boxed{f_m = 2000\,Hz}$

$c(t) = 60\sin(2\pi 100{,}000t)$ comparing with $c(t) = V_c \sin(\omega_c t)$

$\boxed{V_c = 60}$, $\boxed{f_c = 100{,}000\,Hz}$

(i) $m = \frac{V_m}{V_c} = \frac{15}{60} = 0.25$ (iii) $f_m = 2\,KHz$.

$f_c = 100\,KHz$ //



(iii) Carrier $f_c = 100KHz$

USB $f_{USB} = f_c + f_m = 100k + 2k = 102\ KHz$

LSB. $f_{LSB} = f_c - f_m = 100k - 2k = 98\ KHz$

(25) A Bandwidth of 20MHz is available for AM transmitter. If maximum audio freq to be used is 05KHz, how many stations can broadcast?

Sol: Given $f_m = 5KHz$.

$\Rightarrow BW = 2f_m$

$= 2 \times 5K$

$\boxed{BW = 10KHz}$

↑ Bandwidth required by each station

$\therefore$ No of stations,

$N = \frac{20MHz}{10KHz}$

$\boxed{N = 2000\ Channels}$ (or) stations

(26) An FM signal has a resting freq of 105MHz & highest freq of 105.03MHz when modulated by a signal of freq 5KHz. Determine

(i) Freq deviation (ii) Carrier swing (iii) Modulation index (iv) Lowest freq of FM wave (v) Bandwidth of signal.

Sol: Given $f_c = 105MHz$, $f_h = 105.03MHz$, $f_m = 5KHz$.

(i) Δf $\Delta f = f_h - f_c = 105.03 \times 10^6 - 105 \times 10^6 = 30KHz$

(ii) Carrier swing Carrier swing $= 2\Delta f = 60KHz$.

(iii) Modulation index $\beta = \frac{\Delta f}{f_m} = \frac{30 \times 10^3}{5 \times 10^3} = 6$

(iv) Lowest freq of FM wave $f_L = f_c - \Delta f = 105 \times 10^6 - 30 \times 10^3$

$f_L = 104.97\ MHz$ //.

(v) BW $BW = 2(\Delta f + f_m) = 2(30\times10^3 + 5\times10^3) = 70\ KHz$ //.

(4) When the modulating frequency in FM is 600Hz & modulating voltage is 3V, the modulation index is 10. Calculate the maximum deviation. What is the modulation index when the modulating frequency is reduced to 400Hz & the modulating voltage is changed to 5V.

Sol.

(a) Given $f_m = 600Hz$, $V_m = 3V$, $\beta = 10$

W.K.t maximum deviation,

$\Delta f = \beta f_m = 10 \times 600 = 6KHz$ $\left(\because \beta = \frac{\Delta f}{f_m}\right)$

Also $K_f = \frac{\Delta f}{V_m} = \frac{6\times10^3}{3} = 2KHz/V$ $\left(\because \Delta f = K_f V_m\right)$

(b) $f_m = 400Hz$, $V_m = 5V$, $\beta = ?$

We have, $\Delta f = K_f V_m = 2\times10^3 \times 5 = 10KHz$

Now $\beta = \frac{\Delta f}{f_m} = \frac{10\times10^3}{400} = 25$

(5) A carrier wave of amplitude 3V & frequency 10MHz is frequency modulated by a sinusoidal signal of 6V & freq 5KHz. Find the frequency deviation & BW. Given Constant = 1 KHz/Volt.

Sol

Given $V_c = 3V$, $f_c = 10\times10^6 Hz$, $V_m = 6V$, $f_m = 5KHz$.

$\Delta f = ?$, $BW = ?$ $K_f = 1\ KHz/V$

$\Delta f = K_f V_m = 1\times10^3 \times 6 = 6KHz$.

$BW = 2(\Delta f + f_m)$
$= 11KHz$ //.

(29) An AM broadcasting station broadcasts with an average transmitted power of 200W at a modulation index of 60%. Find the transmission power efficiency & the average power in carrier.

Sol: $P_t = 200W$, $M = 60\% = 0.6$

Carrier Power $P_c = \frac{P_t}{1+\frac{M^2}{2}} = \frac{200}{1+\frac{0.6^2}{2}} = 169.49W$

Transmission power efficiency

$$\eta = \frac{M^2}{2+M^2} = 0.1525 \text{ (or) } 15.25\%$$

(30) The carrier frequency in an FM modulator is 10MHz & modulating freq is 20KHz. What are the first three upper sideband & lower sideband freq?

Sol Given $f_m = 20KHz$, $f_c = 10MHz$

Upper sideband frequencies

(a) $f_{USB_1} = f_c + f_s = 10\times10^6 + 2\times10^3 = 10.002MHz = f_{USB_1}$

(b) $f_{USB_2} = f_c + 2f_s = 10\times10^6 + 2\times2\times10^3 = 10.004MHz = f_{USB_2}$

(c) $f_{USB_3} = f_c + 3f_s = 10\times10^6 + 3\times2\times10^3 = 10.006MHz = f_{USB_3}$

Lower sideband frequencies

(a) $f_{LSB_1} = f_c - f_s = 10\times10^6 - 2\times10^3 = 9.998MHz$

(b) $f_{LSB_2} = f_c - 2f_s = 10\times10^6 - 2\times2\times10^3 = 9.996MHz$

(c) $f_{LSB_3} = f_c - 3f_s = 10\times10^6 - 3\times2\times10^3 = 9.994MHz$

(31) In an FM SIM, when the audio freq is 500Hz & the AF voltage is 2.4V, the frequency deviation is

4.8 KHz. If the AF voltage is now increased to 7.2V, what is the new frequency deviation? If the AF voltage is raised to 10V while the AF is dropped to 200Hz, what is the deviation? Find the modulation index in each case.

Sol:

Given (a) $f_{m_1} = 500Hz$, $V_{m_1} = 2.4V$, $\Delta f_1 = 4.8\,KHz$, $\beta_1 = ?$

(b) $V_{m_2} = 7.2V$, $\Delta f_2 = ?$ $\beta_2 = ?$

(c) $V_{m_3} = 10V$, $\Delta f_3 = ?$, $f_{m_3} = 200Hz$, $\beta_3 = ?$

(a) $\beta_1 = \frac{\Delta f_1}{f_{m_1}} = \frac{4.8 \times 10^3}{500} = 9.6$

(b) $\Delta f_2 = K_f V_{m_2} = 2 \times 10^3 \times 7.2 = 14.4\,KHz$

$K_f = \frac{\Delta f}{V_m} = \frac{4.8 \times 10^3}{2.4} = 2\,KHz/V$

$\beta_2 = \frac{\Delta f_2}{f_m} = \frac{14.4 \times 10^3}{500} = 28.8$

(c) $\Delta f_3 = K_f V_{m_3} = 2 \times 10^3 \times 10 = 20KHz$

$\beta_3 = \frac{\Delta f_3}{f_{m_3}} = \frac{20 \times 10^3}{200} = 100$

(2) A carrier wave of 10V & 10MHz is amplitude modulated by AF signal of 4KHz. Write the eqn of AM wave with modulation of 50%.

Sol: Given $V_c = 10V$, $f_c = 10MHz$, $f_m = 4KHz$, $m = 50\% = 0.5$

AM wave is,

$v(t) = (V_c + V_m \sin \omega_m t) \sin \omega_c t$

$$v(t) = [10 + 5\sin(2\pi \times 4\times10^3 t)]\sin(2\pi \times 10\times10^6 t)$$

(07)

$m = \frac{V_m}{V_c}$

$\Rightarrow V_m = mV_c$

$= 0.5\times10$

$V_m = 5V$

$v(t) = V_c(1 + m\sin\omega_m t)\sin\omega_c t$

$$v(t) = 10[1 + 0.5\sin(2\pi\times4\times10^3 t)]\sin(2\pi\times10\times10^6 t)$$

(08)

$(\omega_m = 2\pi f_m$

$\omega_c = 2\pi f_c)$

$$v(t) = V_c\sin\omega_c t + \frac{mV_c}{2}\cos(\omega_c - \omega_m)t - \frac{mV_c}{2}\cos(\omega_c + \omega_m)t$$

$$v(t) = 10\sin(2\pi\times10\times10^6 t) + \frac{0.5\times10}{2}\cos(2\pi\times10\times10^6 - 2\pi\times4\times10^3)t$$

$$-\frac{0.5\times10}{2}\cos(2\pi\times10\times10^6 + 2\pi\times4\times10^3)t$$

$$\Rightarrow v(t) = 10\sin(2\pi10^7 t) + 2.5\cos[2\pi(10^7 - 4\times10^3)t] - 2.5\cos[2\pi(10^7 - 4\times10^3)t]$$

(33) A 20MHz, 3V carrier is modulated by a 1KHz signal. The maximum freq deviation is 10KHz & the sore modulation index is used for both FM & PM. Write expressions for FM & PM

Sol: Given $f_c = 20\times10^6$ Hz, $V_c = 3V$, $f_m = 1\times10^3$ Hz, $\Delta f = 10\times10^3$ Hz

$$\beta = m_p = \frac{\Delta f}{f_m} = \frac{10\times10^3}{1\times10^3} = 10$$

FM wave, $v(t) = V_c\cos[(2\pi f_c t) + \beta\sin(2\pi f_m t)]$

$$\Rightarrow v(t) = 3\cos[(2\pi\times20\times10^6 t) + 10\sin(2\pi\times10^3 t)]$$

PM wave, $v(t) = V_c\cos(\omega_c t + m_p\cos\omega_m t)$

$$\Rightarrow v(t) = 3\cos[(2\pi\times20\times10^6 t) + 10\cos(2\pi\times10^3 t)]$$

$(\because \omega_m = 2\pi f_m$ & $\omega_c = 2\pi f_c)$

TRANSDUCERS

Syllabus: Introduction, Passive Electrical transducer, Resistive transducer, Resistance thermometer, Thermistor. Linear Variable Differential Transformer (LVDT) Active Electrical Transducer, Piezoelectric transducer, Photoelectric transducer.

* Definition of transducer:

A transducer is a device which converts energy (or) information from one form to another.

(or)

A transducer is a device which converts a physical quantity (or) non electrical quantity (temperature, pressure, displacement, force, sound, light etc) into electrical signal (either voltage (or) current)

Note:

① Classification of transducers:

② Based on the role of transducers:

- Input transducer (instrument transducer)
- output transducer (power transducer)

→ An input transducer can be used as a measurement device.

→ An output transducer delivers output signals like force, torque, pressure (or) displacement when the electrical signal is applied as an input.

③ Based on the operation: (Externally Powered)

- Active transducer (Self-generating) & Passive transducer

→ Active transducers develop the voltage (or) current by absorbing the energy needed from the measurand (input)

Ex: Thermo-couple, Piezo electric transducer, Photo-electric cell & photovoltaic cell.

→ Passive transducer accepts energy from an external source to produce output signals (they may absorb some energy from the measurand) (depend on change in R, L, C)

Ex: Resistance strain gauge, thermistor, Linear Variable differential transformer (LVDT), Hall effect sensor, & photomultiplier tube

© Based on output signal:

● Mechanical transducer & Electrical transducers

→ Mechanical transducer produces mechanical nature signal as its output. (Primary transducer)

→ Electrical transducer produces electrical signals as its output. (Secondary transducer)

(d) Based on the nature of output: ● → Analog transducers
→ Digital transducers

(2) Sensor & transducer:

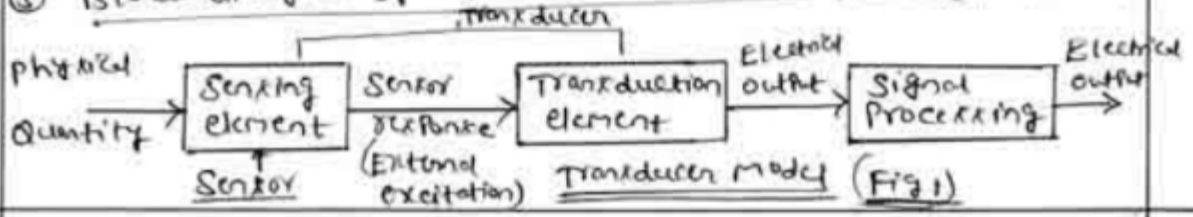
→ Sensor (Primary sensing element) is used to detect any quantity and report it in another form of energy (usually electrical signal)

Ex: Intensity & Luminance of a source may be measured by sensors.

→ Transducer converts a signal from one form to another form of energy (Transduction element) (one type to another type)

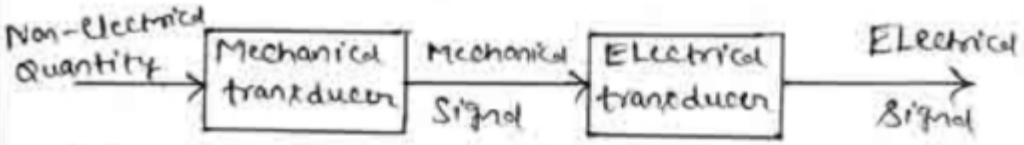
Ex: Temperature is measured by transducers.

(3) Block diagram of transducer model (Fig 1) (Electrical transducer)



Transducer model (Fig 1)

④ Transducers connected in series



Fig②: Transducers connected in series

⑤ Measurands: (Quantity to be measured):

Displacement, Position, Velocity, acceleration, Force, Load, Strain, Rotation, encoding, Vibrations, Flow, Vacuum, temperature, Pressure, Medical imaging, Acoustic fields, Magnetic field, Torque, PH and partial Pressure of O_2 and CO_2 in blood etc

⑥ Advantages & Disadvantages of electrical transducers

→ Advantages

① Amplification & attenuation of electrical signal can be easily done.
② Can be controlled with a very small level of power.
③ Mass-inertia effects are minimized.
④ Effect of friction are minimized.
⑤ The electrical signal can be easily used, transmitted, and processed for the purpose of measurement.
⑥ No mechanical wear and tear.

→ Disadvantages

① Sensors and signal processing circuits are comparatively expensive.
② Less reliable (Sometimes) because of ageing & drift of active components.

(7) Desirable properties of Good transducer (or) Parameters of transducer (or) Requirements of transducer:

(1) Linearity: The input-output characteristics should be linear.

(2) Ruggedness: It should be capable of withstanding overload.

(3) Dynamic response (Dynamic range): It must operate smoothly (uniformly) over a wide range of frequencies.

(4) Repeatability (Precision): It should produce the same output when the same input is applied repeatedly.

(5) Accuracy: It should produce high degree of accuracy

(6) Stability & reliability: The output should be independent of temperature, vibration & other environmental variations. (Error should be minimal)

(7) Residual deformation: It must retain its original shape and structure even after long period of usage.

(8) Physical size: It must have minimal weight & volume

(9) Range: It must cover a different range of measurand values.

(10) Input threshold: It must be possible to detect smallest value of the measurand quantity.

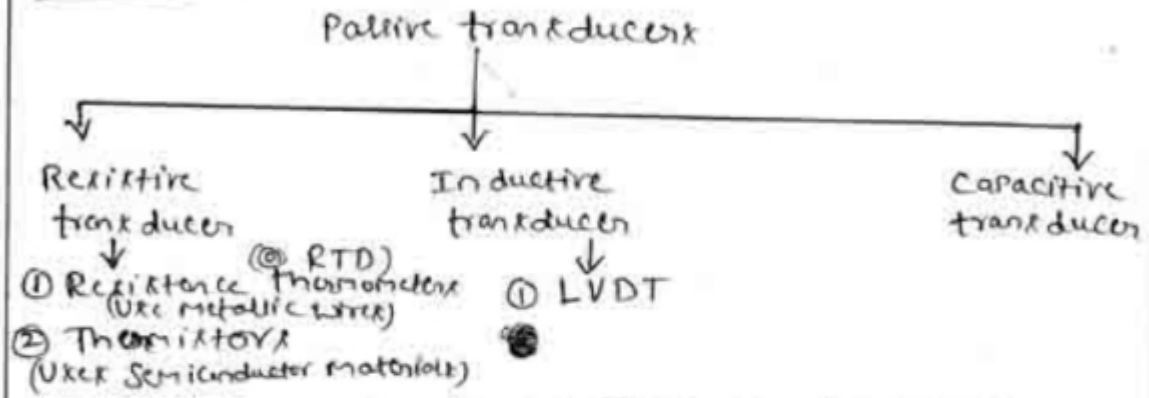
(11) Resolution: It should detect a small change in the measurand quantity.

(12) Loading effects: No loading effect should happen.

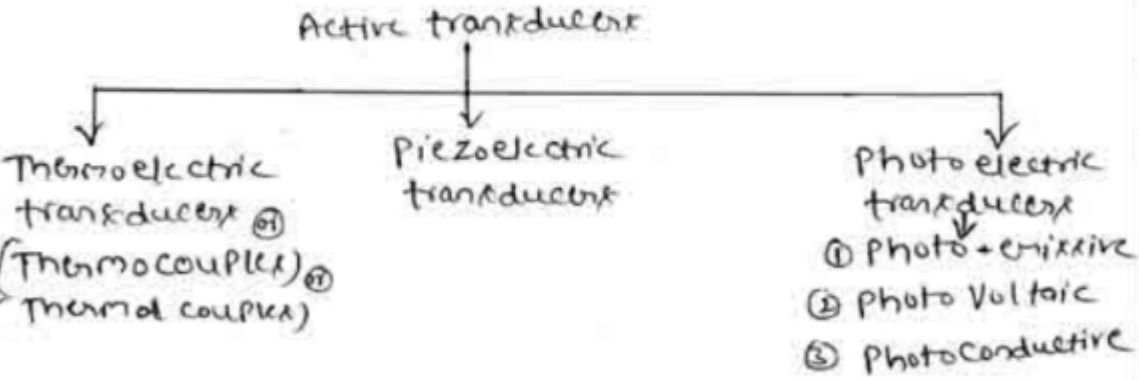
(13) Cost: It should be cost-effective.

* Electrical transducers

① Passive electrical transducers : The transducers that are based on the variation of the parameters (Resistance, Capacitance & Inductance) due to the application of any external stimulus are known as passive transducers



② Active electrical transducers: The transducer which produces output without external source are known as active transducers.



* Passive electrical transducers:

① Resistive transducers:

→ Resistive transducers are passive transducers, in which the resistance changes due to change in physical quantity sensed (measurand)

→ (DC resistance) Resistance of any metal conductor is given by,

$$R = \frac{\rho L}{A} \ (\Omega)$$

Where, (or Specific resistivity)

ρ → Resistivity or Specific resistance of the conductor (Ω-m)

L → Length of conductor (m)

A → Cross-Sectional area of conductor (m^2)

→ Change in resistance occurs when the external stimulus (or Physical phenomenon or input signal or measurand) affects (changes) either the dimension (L or A) or the resistivity (ρ) of the element.

→ **For measurement of displacement, force, pressure, torque etc**

When the resistive elements (conductors) are subjected to pressure, force, torque etc, the dimension (L or A) changes thereby resulting in change in resistance Ex: Strain gauges

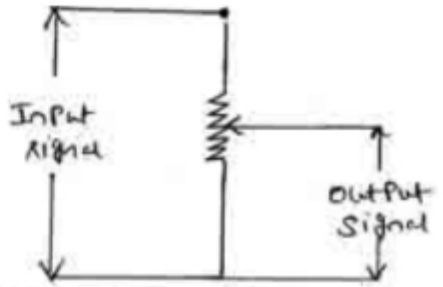
For measurement of temperature

Variation in temperature causes change in the resistivity of the conductor thereby resulting in the change in resistance. Ex: Resistance thermometers.

→ Thermistor & photo conductive transducer rely (work) on changing the concentration of charge carriers.

→ Resistive transducer or Resistive potentiometer consists of a resistive element provided with a sliding contact (wiper).

Motion of sliding contact may be translatory or rotational.



Fig③: Resistive transducer

→ Merits & Advantages

① Easy to operate ② Simple in construction ③ Efficiency is very high ④ Inexpensive ⑤ Both AC and DC can be used ⑥ Speed of response is high ⑦ High resolution ⑧ Available in various sizes.

→ Demerits & Drawbacks & Disadvantages

① A large force is required to move the sliding contact (when potentiometer is used)

② The sliding contact (wiper) can wear out, become misaligned & generate noise.

5) Resistance Thermometers & Resistance temperature detectors (RTD)

→ Construction:

- The wire resistance thermometer usually consists of a coil wound on a mica & ceramic former, as shown in fig ④.
- The coil is wound in bifilar form so as to make it non-inductive. The coils are available in different sizes & with resistance values ranging from 1Ω to 25kΩ
- The resistive element is normally enclosed in a protective tube of pyrex glass, porcelain, quartz & nickel.
- ~~The element is brought~~
- The tube is evacuated and sealed & filled with air & any other inert gas and kept around atmospheric pressure.

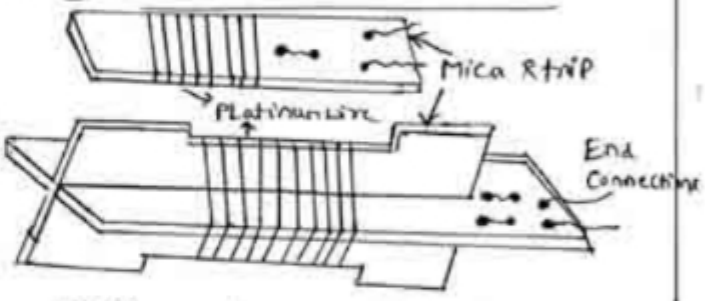


Fig ④: Resistance thermometer

- The element is brought to contact with fluid whose temperature is to be measured.

→ Principle of operation:

- Resistance thermometer is used to measure the temp by measuring resistance in a wire
- The resistance of conductor changes when its temp changes.
- The resistive element is usually made of a solid material, a metal, metallic alloy or a semiconductor.
- Most commonly used materials for resistance thermometers are Platinum, Copper and Nickel.
- Platinum is used (Most stable metal) predominantly.
- The resistivity of the metal increases with temperature (Positive temperature coefficient)
- The resistivity of the semiconductors & insulators generally decreases with temperature (Negative temperature coefficient)
- The resistance R_T of a resistance thermometer at any temperature T(°C) is,

$$R_T = R_0(1+\alpha T)$$

Where, R_0 → Resistance at 0°C (Ω)

T → Temperature in °C

α → Temperature coefficient of resistance (/°C)

$$\alpha = \frac{1}{\Delta T}\frac{\Delta R}{R_0}$$

Where, ΔT → Change in temperature in °C

$\Delta R/R_0$ → Fractional change in resistance.

$\Delta R \rightarrow$ Change in resistance (Ω)

- The Self-heating coefficient E is,

$$E = \frac{\Delta t}{R_T I^2}$$

Where, Δt = (Indicated temperature) − (Fluid (Medium) temperature) (°C)

$R_T \rightarrow$ Resistance of thermometer (Ω)

$I \rightarrow$ Measurement current (A)

- Fig (5) shows the resistance thermometer with Wheatstone bridge.

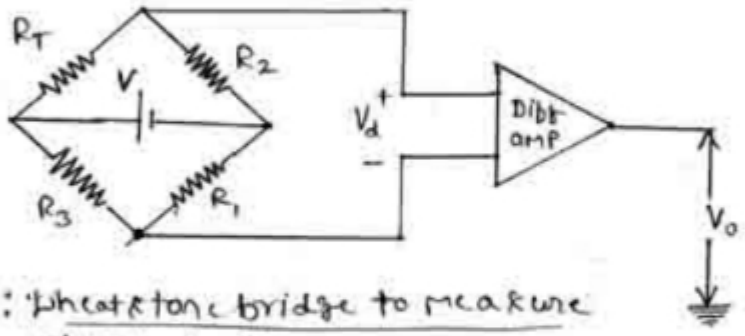


Fig (5): Wheatstone bridge to measure change in R_T

When R_T changes due to change in temperature, the bridge is imbalanced, generating a voltage V_d which is amplified and measured.

- The three main categories of RTD are

① Thin film ② Wire-wound & ③ Coiled elements

→ Advantages:

① High accuracy ② Excellent stability ③ Excellent Precision ④ Linear temperature–resistance characteristics ⑤ Fast (Rapid) response ⑥ Does not require temperature Compensation ⑦ Easy install ⑧ Wide operating range ⑨ Low drift

→ Disadvantages:

① Expensive ② Requires bridge circuit and external power source ③ Possibility of self-heating ④ Large size ⑤ Lower sensitivity ⑥ Tends to drift years of use

(5) Thermistor: → Symbol:

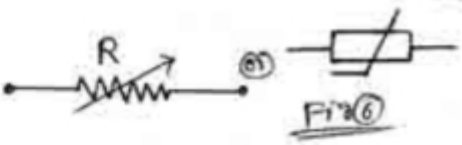
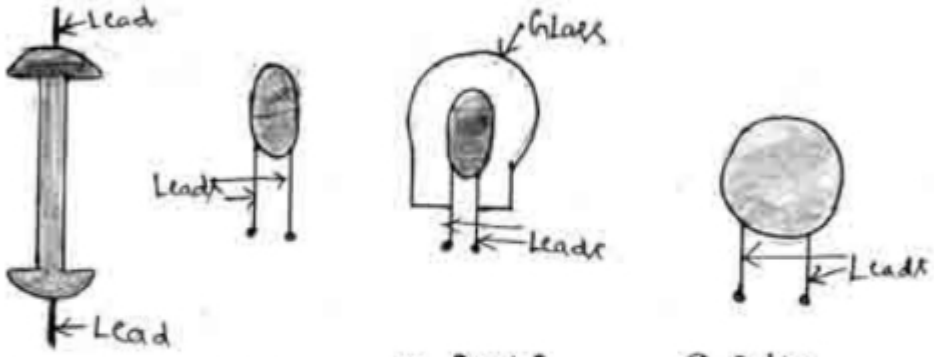


Fig ⑥

→ Construction:

- Thermistors are made up of oxides of Cobalt, nickel, copper, iron, uranium and manganese.
- Different structures of thermistor are shown in fig ⑦



ⓐ Rod ⓑ Bead ⓒ Probe ⓓ Disc

Fig ⑦: Different structures of thermistors

- ⓐ Rod: Diameter → 1.25mm – 4.25mm
  Length → 12.5mm – 50mm
  ⓑ Bead: Diameter → 0.15mm
  ⓒ Probe: Bead with glass coating
  ⓓ Disc: Diameter → 10mm

→ Principle of operation:

→ Thermistor word is derived from THERMally sensitive reSISTOR (not metals).

→ Thermistor is a two terminal semiconductor slab whose resistance decreases with increase in temperature unlike a metal. (negative temperature coefficient)

→ Fig ⑧ shows the temperature – resistance characteristic of a thermistor.

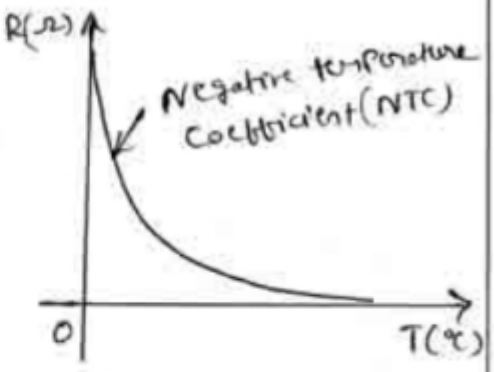


Fig ⑧

→ Thermistor has very high NTC (3–5% per °C)

→ The resistance of the thermistor is (at T(K))

$$R = R_0 e^{\beta\left(\frac{1}{T} - \frac{1}{T_0}\right)} \quad -①$$

Where, R_0 → Resistance at T_0(K)

β → Constant to be determined experimentally.

If T is large, then eqn ① reduces to.

$$R = R_0 e^{\beta/T} \quad -②$$

→ Applications:

① Thermistors are used in the measurement of
(a) Temperature (b) Flow & Pressure (c) Liquid level
(d) Voltage & Power (e) Vacuum (f) Thermal conductivity.

② It can be used as current limiting devices for circuit protection (as replacement for fuses)

③ Used as timers

④ Used as heater in automative industry to provide additional heat inside cabin with diesel engine

⑤ Used as temperature compensated Synthesizer Voltage Controlled oscillators.

⑥ Used in consumer appliances (coffee makers, hair dryers etc)

⑦ Military ⑧ Medical electronics etc

→ Advantages

① Cost effective (Low cost)
② Small size
③ Fast response over a narrow temperature range
④ Good sensitivity (Sense very small changes in temp)
⑤ Higher accuracy
⑥ Rugged
⑦ Flexibility in configuration
⑧ Chemically stable

→ Disadvantages

① Temperature - resistance characteristic is non-linear.
② Not suitable for wide temperature range.
③ Need of shielded cables due to high resistance.
④ Self-heating
⑤ Moisture failures (Non-glass only)

Note:

① Comparision between Resistance thermometers (RTD) & thermistor

Parameter	Resistance thermometer	Thermistor.
① Principle of operation	Positive temperature of coefficient	Negative temperature of coefficient
② Characteristic	Linear	Non-linear (Exponential)
③ Sensitivity	Medium	High
④ Material	Pure metals (Platinum, copper & Nickel)	Ceramic & Polymer (Copper, iron, manganese etc)
⑤ Temperature range	Large (-200 to 650°C)	Limited (-100 to 325°C)
⑥ Accuracy	High	Moderate
⑦ Cost	High	Low

(8) Size	Large	Small
(9) Response Speed	High	High over a various temperature range
(10) Type	Passive	Passive
(11) Power required	Constant Voltage (or) Current	Constant Voltage (or) Current
(12) Self-heating	No (Possibility Less)	Yes
(13) Rugged	No	Yes
(14) Packages	Not FLexible	FLexible

(2) Important Parameters

(a) Time constant: Time for resistance to fall from final value to 63% of the final value (Range: 1-50s)

(b) Dissipation factor: Power dissipated in watt / °c temperature (Range : 1-10mW/°c)

(c) Resistance ratio: Ratio of the resistance at 20°c to resistance at 125°c (Range: 3-60)

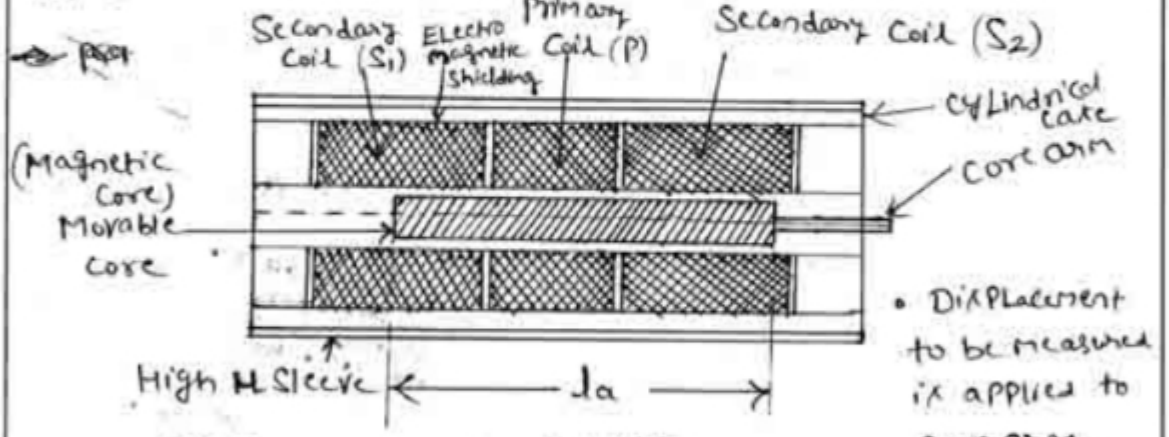
(1) Inductive transducer:

LVDT (Linear Variable Differential Transformer):

- LVDT works under the principle of mutual induction
- LVDT is a type of inductive transducer (electrical transformer) used for measuring displacement. (non-electrical energy (displacement) is converted into an electrical energy)
- Here the inductance is varied according to the physical Quantity to be measured (measurand) (or) displacement

→ Construction: (Fig 9)

- LVDT consists of a primary coil (P), uniformly wound over a certain length of the plastic cylindrical former and two identical secondary coils symmetrically wound on either side of the primary coil and away from the centre.
- The secondary coils (Equal no of turns) are connected in series but in phase opposition so that the output voltage (V_0) will be difference between the individual voltages (V_{01} & V_{02}) induced in the secondary coils (hence the name differential transformer).
- A soft iron core (ferrite rod) is kept inside the plastic former & is free to move inside the former in either direction from the central (null) position.



Fig(9) : Construction of LVDT

→ Principle of operation (Working):

- When an AC voltage (50 Hz to 20KHz) is applied to the primary coil, an alternating magnetic field is induced, which in turn induces voltages (emf) in the secondary coils whose value depends on the core position.
- Let us consider three cases:

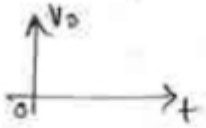
Case 1: (Fig 10)

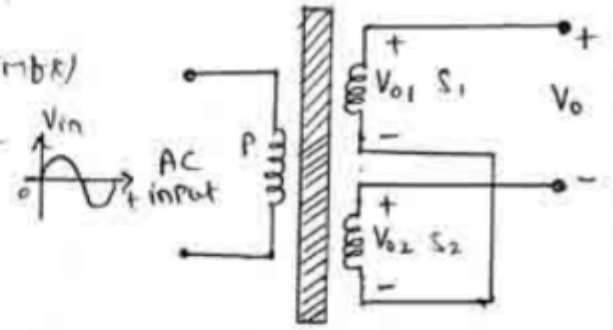
The induced voltages (Emf) in secondary windings are equal. ($V_{o1} = V_{o2}$)

∴ Output voltage V_o is,

$V_o = V_{o1} - V_{o2}$

$\boxed{V_o = 0}$





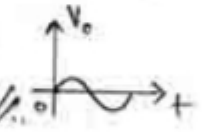
Fig(10): Core in Centre Position

Case 2: (Fig 11)

The induced voltage (Emf) in secondary coil (S_1) is greater than emf in secondary coil (S_2). ($V_{o1} > V_{o2}$)

∴ output voltage V_o is,

$\boxed{V_o = V_{o1} - V_{o2} \text{ (Positive)}}$



Fig(11): Core towards Secondary coil (S_1)

Case 3: (Fig 12)

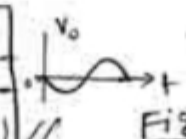
The induced voltage (emf) in secondary coil (S_2) is greater than emf in secondary coil (S_1). ($V_{o2} > V_{o1}$)

∴ Out Put Voltage V_o is,

$\boxed{V_o = V_{o2} - V_{o1} \text{ (Positive)}}$

(or)

$\boxed{V_o = V_{o1} - V_{o2} \text{ (negative)}}$



Fig(12): Core towards Secondary coil (S_2)

- The transfer characteristic of LVDT is shown in fig(13)

→ Applications:

① Used to measure force
② Used to measure weight
③ Used to measure Pressure
④ Used to measure Velocity, acceleration
⑤ Sensing vibrations
⑥ Used in all applications where displacement ranging from fraction millimeter to centimeter.

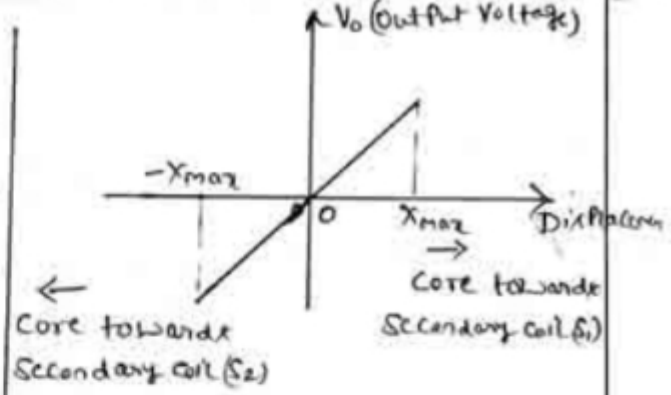


Fig 13: Transfer characteristic of LVDT

→ Advantages:

① Infinite resolution ② Linear ③ High output ④ High sensitivity ⑤ Ruggedness ⑥ Less friction (Less wear & tear) ⑦ Low power consumption ⑧ Low hysteresis ⑨ Good dynamic range ⑩ Relatively low cost ⑪ Robust ⑫ Short response time ⑬ No permanent damage (Exceed the designed range)

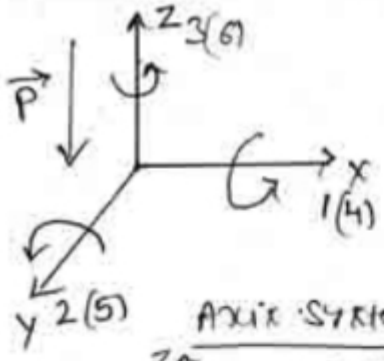
→ Disadvantages:

① Very high displacement is required for generating high voltages.
② Sensitive to magnetic field (Shielding is required)
③ Performance is affected by vibrations.
④ Greatly affected by temperature changes.
⑤ It can only run at speeds up to 1/10 to 1/5 of the excitation frequency (input).

* Active Electrical transducers:

① Piezoelectric transducers: → Construction & Operation

*The ability of certain materials (Crystal & certain Ceramics)



Axis System

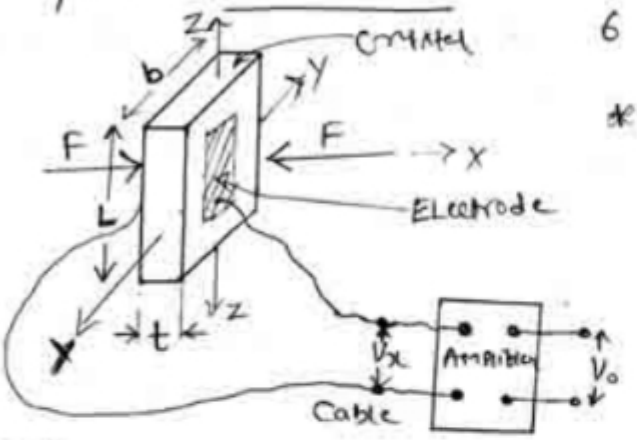


Fig (14): Piezo electric transducer

#	Axis
1	x
2	y
3	z
4	Shear around x
5	Shear around y
6	Shear around z

* Electric Polarization $\vec{P}$ is $\vec{P} = \vec{P}_{xx} + \vec{P}_{yy} + \vec{P}_{zz}$

* The output voltage V_o is,

$$V_o = g t F \text{ (Volts)}$$

$$= g t \frac{F}{A} P \qquad \left[g = \frac{K}{t} \right]$$

Where,

g → Voltage Sensitivity (VM/N)

F → Force (N)

P → Pressure ($= F/A$) (N/m^2)

A → Area of crystal (m^2)

t → Thickness of the crystal (m)

K → Piezo electric constant

→ Advantages

1. High frequency response
2. Small size
3. High output
4. Light weight
5. Simple signal conditioning
6. Negligible phase shift
7. High mechanical rigidity (Rugged)
8. Linearity
9. Low leakage
10. High sensitivity
11. Wide measuring range
12. Ultra Low noise
13. Reliable & robust
14. Unaffected by external EM fields
15. Polarity sensitive

→ Disadvantages:

1. Cannot measure static conditions
2. Output affected by temp. changes.
3. Output affected by long use or high temperature

to produce electric charges (which in turn produces potential or voltage) when mechanical stress is applied across them is called Piezoelectric effect or Piezoelectricity & such crystals (materials) are called Piezoelectric crystals (Piezoelectric transducers) (Converts mechanical energy into electrical energy)

* The Piezoeffect effect is reversible, ie conversely, if a varying potential is applied to crystal, it will change the dimensions of the crystal.
* Voltage depends on the magnitude & direction of force applied to crystal.
* Materials exhibiting the Piezoelectric phenomenon are Quartz, Rochelle salt, tourmaline, Ammonium Dihydrogen Phosphate (ADP), Lithium Sulphate (LS) & Di Potassium Tartrate (DKT) etc
* The word Piezo- is derived from the Greek word 'Piezein', which means to squeeze or press.
* Types of Piezoelectric materials (tourmaline)
  1. Natural crystals (Ex: Quartz, rochelle salt)
  2. Synthetic crystals (Ex: Lithium Phosphate)
  3. Ferroelectric ceramics (Ex: Barium titanate)
* Based on the direction of force applied, there are three modes of operation.
  1. Thickness expander mode
  2. Length expander mode
  3. Volume expander mode
* Fig (14) shows Piezoelectric transducer.

→ Applications

① It is used to measure force, pressure, acceleration, torque, strain & amplitude of vibration.

② Used in ⓐ Aircraft flight test ⓑ Generation of ultrasonic frequencies ⓒ Gas lighters ⓓ Electronic cigarette Lighters ⓔ Aero-space ⓕ Medicines ⓖ Industry ⓗ Microphones (i) Actuator

② Photo electric transducers:

→ Construction & Working

* If Light is incident on a metal surface, the entire Quantum energy is converted into Kinetic energy of the electron & helps the electron to move & Contribute current in the metal. This is called Photoelectric effect

* According to operating principle, Photoelectric transducers may be grouped as follows.

① Photoemissive ② Photo Voltaic ③ Photo Conductive (resistive)

* Photo emissive cell (Photo emissive transducer) (Photo tube)

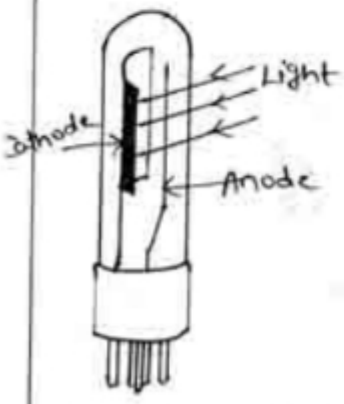


Fig (15): Photoemissive cell

- It consists of Semi-cylindrical (or) V-shaped electrode (cathode) coated with a photo emissive material and an anode (thin wire), both enclosed in an evacuated glass bulb (Fig (15)).
- When the light falls on the cathode, electrons are emitted and are attracted by the anode & hence current flows.
- Current depends on (i) Intensity of incident radiation & (ii) Anode - Cathode Voltage.

* Photo Voltaic cell (Solar Cell)

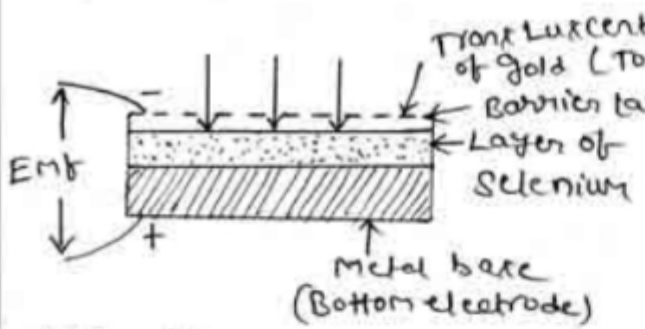


Fig (15): Photo Voltaic transducer (Selenium cell)

- It consists of a metal electrode (Bottom) on which a layer of selenium is deposited, on the top of this a barrier layer is formed which is coated with a very thin layer of gold. (Fig 16)

- When light falls on semiconductor (Selenium), a potential (Voltage) is generated.

* Photo Conductive Cell (or) Photo resistive cell : (or) Light Dependent resistor (LDR)

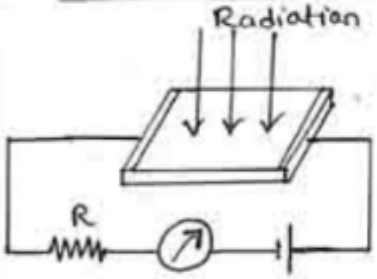


Fig (17): Photo Conductive transducer

- It consists of Semiconductor material (Like Selenium, Cadmium Sulphide, Lead Sulphide and thalmium Sulphide) with two electrodes.

- When the light is illuminated on semiconductor material, its resistance decreases & current through the circuit increases.

→ Advantages

1. Low cost
2. Fast response
3. Sensitivity
4. Energy conversion efficient

→ Disadvantages

1. Incident light must have enough energy to impart to electrons

→ Applications

① Photo-emissive cell

ⓐ Photometry & Colorimetry ⓑ Sound reproduction from a motion-picture film ⓒ on & off circuits ⓓ Automatic opening of door ⓔ Sorting of objects on a conveyor belt.

② Photo-Voltaic cell

ⓐ Automatic Control Systems ⓑ Television circuits
ⓒ Sound Motion Picture and reproducing equipment.
ⓓ Solar vehicles, Solar lamps ⓔ Space craft.

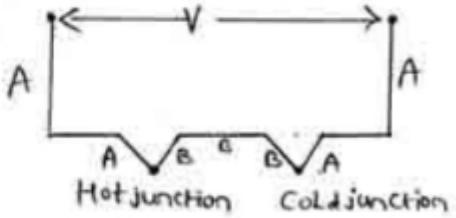
③ Photo-Conductive cell

ⓐ Detection of Ships & Aircrafts ⓑ Telephony by modulated infrared lights ⓒ Optical communication systems
ⓓ object counting in industry.

④ Thermoelectric transducers ⓐ Thermo Couples ⓑ Thermal Couples:

→ It converts thermal energy ⓐ heat energy into electrical energy & vice versa.

→ It consists of two wires of different metals, joined together to form two junctions as shown in fig①.



A: Metal A
B: Metal B

Fig①: Thermo Couple

→ one of the two junctions is called the hot junction & the other is cold junction (reference junction)

→ There are four physical effects that contribute to the output voltage of the thermocouple.

ⓐ Seebeck effect
ⓑ Peltier effect
ⓒ Thomson effect
} Thermodynamically reversible effects

ⓓ Joule heating → Irreversible thermoelectric effect

ⓐ Seebeck effect:

→ It is the conversion of heat directly into electricity at the junction of different types of wire (at different temperatures)

→ In 1821, the German physicist Thomas Johann Seebeck discovered that a compass needle would be deflected by a closed loop formed by two different metals joined in two places, with a temperature difference between the joints (because of magnetic field)

→ Emf is given by,

$$E_{emf} = -S \nabla T$$

Where, S → Seebeck effect @ Thermopower (−100 μV/K to 1,000 μV/K)

∇T → Gradient in temperature

ⓑ Peltier effect:

→ It is the reverse phenomenon of Seebeck effect

→ It is the conversion of electricity into heat (or cool)

→ The amount of heat liberated @ absorbed is proportional to the quantity of current that crosses the junction.

→ The amount of heat liberated @ absorbed when one ampere passes for a second is called the Peltier coefficient

→ Peltier heat generated at the junction per unit time is,

$$\dot{Q} = (\Pi_A - \Pi_B) I$$

Where Π_A (Π_B) → Peltier coefficient of conductor A (B)

I → Electric current (from A to B)

ⓒ Thomson effect:

→ It is also the reverse phenomenon of Seebeck effect.

→ It is the conversion of electricity into heat

→ Ex: When a current flows through a copper conductor, having thermal gradient (temperature difference) along its length, heat is liberated at any point where the current is in the same direction as the heat flow, while heat is absorbed at any point when the current flows in the direction opposite to the flow of heat.

→ Heat production rate per unit volume.

$$\dot{Q} = -K J \cdot \nabla T$$

K → Thomson coefficient

∇T → Temperature gradient

J → current density.

→ First Thomson relation is,

$$K = \frac{d\pi}{dT} - S$$

Applications of thermocouple

Steel industry, gas-fed heating, Thermoelectric refrigerator & generator, measurement of temperature and radiation.

ⓓ Joule heating:

→ It is irreversible thermoelectric effect.

→ Heat is generated whenever a current is passed through a resistive material.

→ The electric current 'I' is transformed into heat 'P' according to,

$$P = RI^2$$

where, P → Power (W)

R → Electrical resistance of the conductor (Ω)

I → Electric current (A).

Problems

① In a Linear Voltage differential transformer (LVDT) the output voltage is 1.8V at maximum displacement. At a certain load the deviation from linearity is maximum and is ± 0.0045V from a straight line through the origin. Find the linearity at the given load.

Sol: Given $V_o = 1.8V$, $\Delta V = \pm 0.0045V$

$$\therefore \text{Linearity} = \frac{\Delta V}{V_o} = \frac{\pm 0.0045}{1.8} = \pm 0.0025 = \pm 0.25\%$$

② A Piezoelectric crystal measuring 6mm × 6mm × 1.8mm is used to measure force. Its voltage sensitivity is 0.055 Vm/N. Calculate the force if voltage developed is 120V.

Sol: Given $A = 6mm \times 6mm$, $t = 1.8mm$,

$g = 0.055 Vm/N$, $V_o = 120V$

We know $V_o = gtP$

$$\Rightarrow P = \frac{V_o}{gt} = \frac{120}{0.055 \times 1.8 \times 10^{-3}} = 1.212 \text{ MN/m}^2$$

$\therefore$ Force, $F = PA = 1.212 \times 10^6 \times 6 \times 10^{-3} \times 6 \times 10^{-3}$

$$F = 43.63N$$

① Equation of Straight line.

ⓐ $y = mx + c$ ⓑ $\frac{y_2 - y_1}{y - y_1} = \frac{x_2 - x_1}{x - x_1}$ ⓒ $\frac{x}{a} + \frac{y}{b} = 1$

ⓓ $y = mx$ ⓔ $y - y_1 = m(x - x_1)$ ⓕ $x\cos\theta + y\sin\theta = p$

ⓖ $Ax + By + C = 0$

②

$\cos 2\theta = 1 - 2\sin^2\theta$, $\cos 2\theta = 2\cos^2\theta - 1$

$\cos 2\theta = \cos^2 x - \sin^2 x$

③

$\int \sin\theta \, d\theta = -\cos\theta$. $\int \cos\theta = \sin\theta$, $\int t \, dt = \frac{t^2}{2}$

$\int k \, dt = kt$

④

$\cos 0 = 1$, $\cos \pi/2 = 0$, $\cos\pi = -1$, $\cos 3\pi/2 = 0$, $\cos 2\pi = 1$

$\sin 0 = 0$. $\sin 90^\circ = 1$, $\sin 180^\circ = 0$, $\sin 270 = -1$, $\sin 360^\circ = 0$

⑤

$\frac{\text{Any finite non-zero}}{\infty} = 0$

⑥

$\frac{d}{dt}(\sin t) = \cos t$ $\frac{d}{d\theta}(\sin n\theta) = n\cos n\theta$

$\frac{d}{dt}(\cos nt) = -n\sin nt$, $\frac{d}{dt}(t) = 1$, $\frac{d}{dt}(k) = 0$

⑦

$\sin(A+B) = \sin A\cos B + \cos A \sin B$

$\sin(A-B) = \sin A\cos B - \cos A \sin B$

$\cos(A+B) = \cos A\cos B - \sin A \sin B$

$\cos(A-B) = \cos A\cos B + \sin A \sin B$

$\sin A \sin B = \frac{1}{2}[\cos(A-B) - \cos(A+B)]$

$\cos A \cos B = \frac{1}{2}[\cos(A+B) + \cos(A-B)]$

$\sin A \cos B = \frac{1}{2}[\sin(A+B) + \sin(A-B)]$

(5)

K – Kilo – 10^3

M – Mega – 10^6

G – Giga – 10^9

m – milli – 10^{-3}

μ – Micro – 10^{-6}

n – nano – 10^{-9}

p – Pico – 10^{-12}

f – femto – 10^{-15}

Formulae : Introduction

① Mass of Proton = Mass of neutron = 1.672×10^{-27} kg

② Mass of electron = 9.1×10^{-31} kg

③ Charge of an electron = -1.602×10^{-19} c

④ Charge of Proton = 1.602×10^{-19} c

⑤ Atomic weight @ Atomic mass = Number of Protons + Number of Neutrons

⑥ Atomic number = Number of Protons @ electrons

⑦ Amount of energy emitted @ absorbed = $W_2 - W_1 = hf$ (Joule)

⑧ Planck's constant, $h = 6.626 \times 10^{-34}$ Js

⑨ Energy of an electron, $E_n = -21.76 \times 10^{-19} \frac{Z^2}{n^2}$ (Joule)

@

$= -\frac{21.76 \times 10^{-19}}{1.6 \times 10^{-19}} \frac{Z^2}{n^2}$ @ $-\frac{13.6 Z^2}{n^2}$ (eV)

⑩ 1 eV $= 1.602 \times 10^{-19}$ Joule

⑪ conductance, $G = \frac{1}{R}$ S @ mho @ Ω, R → Resistance (Ω)

⑫ Conductivity $\sigma = \frac{1}{\rho}$ S/m @ Ω/m, ρ → Resistivity (Ωm)

⑬ KCL: $\sum I = 0$

⑭ KVL: $\sum V + \sum IR = 0$

⑮ RMS Voltage, $V_{rms} = \frac{V}{\sqrt{2}}$

⑯ Angular frequency $\omega = 2\pi f$ (rad/s)

f → Linear frequency (cycle/s) @ (Hz)

(B) Pressure $P = \frac{\text{Force}}{\text{Area}}$

① $V_\gamma = \begin{cases} 0.3V & \text{for Ge} \\ 0.7V & \text{for Si} \end{cases}$, $I_0 = \begin{cases} 1\mu A & \text{for Ge} \\ 100nA & \text{for Si} \end{cases}$, $V_{BR} = \begin{cases} 50V & \text{for Ge} \\ 75V & \text{for Si} \end{cases}$

② (Decrease) Change in Barrier Voltage. (for Ge & Si).

$$\Delta V_\gamma = -0.002 \Delta t$$

Where, $\Delta t \rightarrow$ (Increase) in temperature (in °C)

③ Diffusion capacitance,

$$C_D = \frac{\tau I_F}{V_F} = \frac{\tau I_F}{\eta V_T}$$

Transition capacitance

$$C_T = \frac{K}{(V_a - V)^n}$$

④ Reverse current at T_2 is,

$$I_0(T_2) = I_0(T_1)\left[2^{(T_2-T_1)/10}\right]$$

⑤ Shockley equation,

$$I_D = I_0(e^{V_D/\eta V_T} - 1), \quad \eta = \begin{cases} 1 & \text{for Ge} \\ 2 & \text{for Si} \end{cases}$$

⑥

$$V_D = \eta V_T \ln\left(\frac{I_D}{I_0} + 1\right)$$

$$V_T = \frac{kT}{q}, \quad k = 1.38 \times 10^{-23} J/K$$

$$T(K) = 273 + T(°C)$$

⑦ Power, $P = VI = I^2R = V^2/R$

⑧ Minimum fall time, $t_{f(min)} = 10\, t_{rr}$.

$t_{rr} \rightarrow$ Reverse recovery time

⑨ Power dissipation at T_2(°C),

$$P_2 = P_1(\text{at } T_1) - D \times \Delta T$$

$D \rightarrow$ Derating factor (W/°C)

$\Delta T \rightarrow (T_2 - T_1)$

⑩ Diode Voltage drop at any temperature (T_2°C),

$$V_{F_2} = V_{F_1}(\text{at } T_1) + [\Delta T \ (\Delta V_F/^\circ C)]$$

$\Delta V_F/^\circ C \rightarrow$ { -1.8 mV/°C for Si ; -2.02 mV/°C for Ge }

(10) Dynamic resistance of a forward biased diode at any temperature. (Sometimes called as Pure ac resistance)

$$r_d' = \frac{26\text{mV}}{I_F}\left(\frac{T+273^\circ C}{298^\circ C}\right)$$

(11) Dynamic forward resistance (from characteristics).

$$r_d = \frac{\Delta V_F}{\Delta I_F} = \frac{1}{\text{Slope of forward characteristics}} = \frac{V_{F_2}-V_{F_1}}{I_{F_2}-I_{F_1}}$$

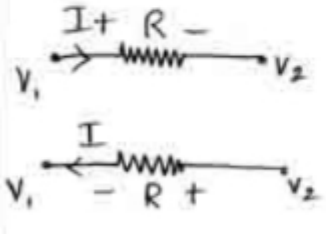
(12) Semiconductor substrate resistance.

$$r_{substrate} = r_d - r_d'$$

(13) DC or Static resistance

$$R_F = \frac{V_F}{I_F} \qquad R_R = \frac{V_R}{I_R}$$

(14)



$$I = \frac{V_1 - V_2}{R} \qquad I = \frac{V_2 - V_1}{R}$$

(Ohm's law $V = IR$ or $I = V/R$)

(15) DC load line end Points

$$A(V,0) = A(V_F, 0) \qquad B(0, I_F) = B\left(0, \frac{V}{R}\right)$$

(16) $$\text{TUF} = \frac{\text{DC Power delivered to load}}{\text{AC rating of the transformer secondary}}$$

For HWR, TUF = 0.287, For FWR, TUF = 0.693.

For FWBR : TUF = 0.812

(i) Instantaneous secondary voltage of transformer.

$$V_2 = \frac{N_2}{N_1} V_1 = \frac{N_2}{N_1} V_m \sin \omega t$$

(ii) HWR ($R_s = 0$)
Current through diode.

$$i_o = \begin{cases} I_m \sin \omega t & ; 0 \le \omega t \le \pi \\ 0 & ; \pi \le \omega t \le 2\pi \end{cases}$$

(iii) Peak load current. $I_m = \frac{V_m}{R_f + R_L}$

(iv) $I_{dc} = \frac{I_m}{\pi}$, $V_{dc} = \frac{V_m/\pi}{1 + R_f/R_L}$, $V_{rms} = \frac{V_m/2}{1 + R_f/R_L}$, $I_{rms} = \frac{I_m}{2}$

$\eta = 121\%$, $\eta = \frac{V_{ac}}{V_{dc}} = \frac{I_{ac}}{I_{dc}}$, $I_{rms}^2 = I_{dc}^2 + I_{ac}^2$

$V_{rms}^2 = V_{ac}^2 + V_{dc}^2$, $\eta = \frac{P_{ac}}{P_{dc}} = \frac{40.6\%}{1 + R_f/R_L}$, $P_{IV} = V_m$

% Regulation $= \frac{R_f}{R_L} \times 100$, $f_{out} = f_{in}$.

Ideally, $R_f = 0$

FWCTR (Assuming transformer secondary resistance (R_s) = 0)

(v) $i_o = I_m \sin \omega t$, $0 \le \omega t \le \pi$, $I_m = \frac{V_m}{R_f + R_L}$

$I_{dc} = \frac{2I_m}{\pi}$, $V_{dc} = \frac{2V_m/\pi}{1 + R_f/R_L}$, $I_{rms} = \frac{I_m}{\sqrt{2}}$, $V_{rms} = \frac{V_m/\sqrt{2}}{1 + R_f/R_L}$

$\eta = 48.3\%$, $\eta = \frac{81.2\%}{1 + R_f/R_L}$, % Regulation $= \frac{R_f}{R_L} \times 100$

PIV $= 2V_m$, $f_{out} = 2 f_{in}$.

FWBR (Assuming $R_s = 0$)

22) $i_o = I_m \sin \omega t : 0 \le \omega t \le \pi$. $I_m = \dfrac{V_m}{2R_f + R_L}$

$I_{dc} = \dfrac{2I_m}{\pi}$. $V_{dc} = \dfrac{2V_m/\pi}{1 + 2(R_f/R_L)}$. $I_{rms} = \dfrac{I_m}{\sqrt{2}}$.

$V_{rms} = \dfrac{V_m/\sqrt{2}}{1 + 2(R_f/R_L)}$. $\gamma = 48.3\%$. $\eta = \dfrac{81.2\%}{1 + 2(R_f/R_L)}$

% Regulation $= \dfrac{2R_f}{R_L} \times 100$. $PIV = V_m$. $f_{ou} = 2 f_{in}$.

2) Reactance of a capacitor, discharging time

$X_c = \dfrac{1}{2\pi f c}$ $\qquad t_d = C R_L$

3) HWR with 'C' filter

$\gamma = \dfrac{1}{2\sqrt{3} f R_L C}$. $V_{r(p-p)} = \dfrac{I_{dc}}{fC} = \dfrac{V_{dc}}{fCR_L}$

$V_{dc} = V_m - \dfrac{I_{dc}}{2fc} = V_m - \dfrac{V_{dc}}{2fcR_L} = \dfrac{V_m}{\left(1 + \dfrac{1}{2fcR_L}\right)}$

5) FWCTR & FWBR with 'C' filter

$\gamma = \dfrac{1}{4\sqrt{3} f R_L C}$. $V_{r(p-p)} = \dfrac{I_{dc}}{2fc} = \dfrac{V_{dc}}{2fcR_L}$

$V_{dc} = V_m - \dfrac{I_{dc}}{4fc} = V_m - \dfrac{V_{dc}}{4fcR_L} = \dfrac{V_m}{1 + \dfrac{1}{4fcR_L}}$

28) Zener diode voltage regulator (no load)

$I_{zk} < I_z < I_{zm}$. $R_1 = \dfrac{V_s - V_z}{I_z}$. $P_{R_1} = I_z^2 R_1$

$I_{z\min} = \dfrac{V_{s\min} - V_z}{R_1}$. $I_{z\max} = \dfrac{V_{s\max} - V_z}{R_1}$. $V_o = V_z$

(7) Zener diode voltage regulator (with load)

$I_1 = I_Z + I_L$, $I_1 = \frac{V_S - V_Z}{R_1}$, $I_1 = I_{Z\min} + I_{L\max}$.

$I_1 = I_{ZM}$, $I_{ZM} = I_{Z\min} + I_{L\max}$, $I_{ZM} = \frac{V_S - V_Z}{R_1}$

$R_1 = \frac{V_S - V_Z}{I_{ZM}}$

$I_Z = \left(\frac{V_S - V_Z}{R_1}\right) - I_L$, $R_{1(\max)} = \frac{V_{S\min} - V_Z}{I_{Z\min} + I_{L\max}}$

$R_{1(\min)} = \frac{V_{S\max} - V_Z}{I_{Z\max} + I_{L\min}}$, $I_{ZT} = 20mA$, $I_{Z\min} = 5mA$

(8) Source effect = ΔV_o for a 10% change in V_S

Line regulation = $\frac{\Delta V_o \text{ for a 10\% change in } V_S}{V_o} \times 100\%$

(9) Load effect = ΔV_o for $\Delta I_{L(\max)}$

Load regulation = $\frac{\Delta V_o \text{ for } \Delta I_{L(\max)}}{V_o} \times 100\%$

Transistor

(10) $I_E = I_B + I_C$, $I_{BE} = \begin{cases} 0.3V \text{ for Ge} \\ 0.7V \text{ for Si} \end{cases}$ $V_{CE} = 3 \text{ to } 20V$

(11) $I_C = \alpha I_E + I_{CBO} = \frac{\alpha}{1-\alpha} I_B = \beta I_B + I_{CEO}$

$I_{CEO} = (1+\beta) I_{CBO}$

(12) $h_{fb} = \alpha = \frac{I_C}{I_E}$, $\beta = \frac{I_C}{I_B} = h_{fe}$, $\gamma = \frac{I_E}{I_B} = h_{fc}$

$\alpha = \frac{\beta}{1+\beta}$, $\beta = \frac{\alpha}{1-\alpha}$, $\gamma = 1+\beta$, $\beta = \gamma - 1$

$\alpha = \frac{\gamma - 1}{\gamma}$, $\gamma = \frac{\beta}{\alpha}$

(ii) $R_i = \left.\frac{\Delta V_{in}}{\Delta I_{in}}\right|_{V_{out} = \text{Constant}}$

$R_o = \left.\frac{\Delta V_{out}}{\Delta I_{out}}\right|_{I_{in} = \text{Constant}}$

(iii) $P_{D(max)}(T_2°C) = P_{D(max)}(T_1°C) - DF(T_2 - 25)$

(iv) $A_v = \frac{V_{out}}{V_{in}}$

(v) $0 \leq \alpha \leq 1$ $\quad \beta > 1$

BJT Biasing

① **Stability factor**

$$S = \frac{dI_c}{dI_{co}} \text{ at constant } I_B \text{ \& } \beta$$

② $V_{BE} = \begin{cases} 0.3\,V \text{ for Ge} \\ 0.7\,V \text{ for Si} \end{cases}$, $V_{CE} = \begin{cases} 0.5\,V \text{ for Ge} \\ 1\,V \text{ for Si} \end{cases}$

③ **DC load line end Points**

$$A(V_{CE}, 0) = A(V_{cc}, 0), \quad B(0, I_c) = B\left(0, \frac{V_{cc}}{R_c}\right)$$

④ **Base - bias**

$$I_B = \frac{V_{cc} - V_{BE}}{R_B}$$

$$I_c = h_{FE} I_B = \beta I_B$$

$$V_{CE} = V_{cc} - I_c R_c$$

Q Point (V_{CE}, I_c) , $S = 1 + \beta$

Design of Base - bias

(a)	$R_B = \frac{V_{cc} - V_{BE}}{I_B}$
(b)	$I_B = \frac{I_c}{h_{FE}}$
(c)	$R_c = \frac{V_{cc} - V_{CE}}{I_c}$

⑤ **Voltage - divider**

Approximate method

$$I_2 = \frac{V_{cc}}{R_1 + R_2}$$

$$V_B = \frac{V_{cc}}{R_1 + R_2} R_2$$

$$V_E = V_B - V_{BE}$$

$$I_E = \frac{V_B - V_{BE}}{R_E}$$

$V_{CE} = V_{cc} - I_c(R_c + R_E)$, $V_c = V_{cc} - I_c R_c$ & $V_{CE} + V_E$

Exact method

$$V_T = \frac{V_{cc} R_2}{R_1 + R_2}, \quad R_T = \frac{R_1 R_2}{R_1 + R_2}, \quad I_B = \frac{V_T - V_{BE}}{R_T + R_E(1 + h_{FE})}$$

$$I_C = h_{FE} I_B, \quad V_{CE} = V_{cc} - I_C R_C - I_E R_E, \quad V_E = I_E R_E$$

$$V_C = V_{CE} + V_E = V_{cc} - I_C R_C, \quad V_B = V_{BE} + V_E$$

Design of voltage-divider

$$I_2 = \frac{I_C}{10}, \quad V_E >> V_{BE}, \quad R_E = \frac{V_E}{I_C}, \quad R_2 = \frac{V_B}{I_2}, \quad R_1 = \frac{V_{cc} - V_B}{I_2}$$

$$R_C = \frac{V_{cc} - V_{CE} - V_E}{I_C}$$

Q-Point $Q(V_{CE}, I_C)$

Stability factor

$$S = \frac{1 + \beta}{1 + \beta\left(\frac{R_E}{R_E + R_{TH}}\right)}$$

D Base-bias

Percentage change in I_C.

$$\Delta I_C(\%) = \frac{I_C(T_2{}^\circ C) - I_C(T_1{}^\circ C)}{I_C(T_1{}^\circ C)} \times 100$$

Percentage change in V_{CE}

$$\Delta V_{CE}(\%) = \frac{V_{CE}(T_2{}^\circ C) - V_{CE}(T_1{}^\circ C)}{V_{CE}(T_1{}^\circ C)} \times 100$$

Introduction to operational amplifier

1. $V_o = A_d V_d + A_{cm} V_{cm}$ or $A_d V_d \left(1 + \frac{1}{CMRR} \frac{V_{cm}}{V_d}\right)$

   $V_d = V_1 - V_2$, $V_{cm} = \frac{V_1 + V_2}{2}$.

2. $A_d(dB) = 20 \log_{10}(A_d)$, $A_d = \frac{V_o}{V_d} = \frac{V_o}{V_1 - V_2}$

   $A_{cm}(dB) = 20 \log_{10}(A_{cm})$, $A_{cm} = \frac{V_o}{V_{cm}} = \frac{V_o}{(V_1 + V_2)/2}$

3. $CMRR = \frac{A_d}{A_{cm}}$, $I_{io} = |I_1 - I_2|$, $I_{ib} = \frac{I_1 + I_2}{2}$.

4. $SR = \left.\frac{dV_o}{dt}\right|_{max} = (2\pi V_m) f_{max} = V_m(\omega_{max})$ or $f_{max} = \frac{SR}{2\pi V_m}$

   or $\omega_{max} = \frac{SR}{V_m}$

5. $SVRR\ (PSRR) = \frac{\Delta V_{io}}{\Delta V}$

6. Virtual ground concept: $V_1 = V_2$

7. Voltage follower $V_o = V_i$, $A_v = 1 = \frac{V_o}{V_i}$

8. Inverting amplifier

   $V_o = -\left(\frac{R_f}{R_1}\right) V_i$, $A_v = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$

9. Non-inverting amplifier

   $V_o = \left(1 + \frac{R_f}{R_1}\right) V_i$, $A_v = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}$

10. Inverting summer

    $V_o = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \cdots + \frac{R_f}{R_n} V_n\right)$

11) Non-inverting Summer

$$V_o = \frac{(1+R_f/R)}{(1+R_1/R_2)} V_1 + \frac{(1+R_f/R)}{(1+R_2/R_1)} V_2$$

12) Subtractor

$$V_o = V_2 - V_1 \text{ or } \frac{R_f}{R}(V_2 - V_1)$$

13) Differentiator

$$V_o = -RC \frac{dV_i}{dt}$$

14) Integrator

$$V_o = -\frac{1}{RC} \int_0^t V_i \, dt + V_o(0)$$

15) Total gain of a circuit consisting of two circuits with gains A_1 & A_2 is,

$$A = A_1 A_2$$

16) Input currents of an op-amp.

$$I_1 = I_{ib} + \frac{I_{io}}{2} \qquad I_2 = I_{ib} - \frac{I_{io}}{2}$$

17) $V_1 \rightarrow i \; C \; \leftarrow V_2$ $\qquad i = C \frac{d(V_1 - V_2)}{dt}$

1) NOT gate, AND gate, OR gate, NAND gate, NOR gate

$Y = \bar{A}$ $Y = AB$ $Y = A+B$ $Y = \overline{AB}$ $Y = \overline{A+B}$

EX-OR gate EX-NOR gate

$Y = \bar{A}B + A\bar{B}$ (or) $\overline{A\bar{B} + AB}$

$Y = \overline{\bar{A}\bar{B} + AB}$ (or) $\bar{A}B + A\bar{B}$

2) Boolean laws

$1 \cdot A = A$, $0 \cdot A = 0$, $A \cdot A = A$, $A \cdot \bar{A} = 0$, $AB = BA$

$(AB)C = A(BC)$, $A + BC = (A+B)(A+C)$, $A(A+B) = A$

$0 + A = A$, $1 + A = 1$, $A + A = A$, $A + \bar{A} = 1$, $A + B = B + A$,

$(A+B)+C = A+(B+C)$, $A(B+C) = AB + AC$, $A + AB = A$.

$\bar{\bar{A}} = A$, $\bar{0} = 1$, $\bar{1} = 0$

3) De-Morgan's Laws

$\overline{A+B+C+\cdots+N} = \bar{A} \cdot \bar{B} \cdot \bar{C} \cdots \bar{N}$

$\overline{ABCD\cdots N} = \bar{A} + \bar{B} + \bar{C} + \bar{D} + \cdots + \bar{N}$

4) Half adder

Sum, $S = \bar{A}B + A\bar{B} = A \oplus B$

Carry, $C = AB$

5) Full adder

Sum, $S = A \oplus B \oplus C_{in} = (\bar{A}B + A\bar{B})C_{in} + (\bar{A}\bar{B} + AB)C_{in}$

Carry, $C_{out} = (A \oplus B)C_{in} + AB = (\bar{A}B + A\bar{B})C_{in} + AB$

② Rules to be followed to simplify the Boolean expression

Rule 1 : ⓐ Convert POS (Product of Sum) term to SOP (Sum of Product) [If no complement @ a complement on full logic expression is present]

ⓑ If complement is present for few terms : Use demorgan's laws, then follow Rule 1 ⓐ

Rule 2 : ⓐ Use Boolean algebra laws.

ⓑ If any common variable are there among few terms @ all the terms, then take it outside

ⓒ Repeat Rule 2 ⓐ

③ Rules to be followed to implement using only NAND gate

Step 1 : Follow the above Rules (1 to 2)

Step 2 : ⓐ Make sure no '+' is present (only '·' is allowed)

ⓑ If '+' (OR) is present, Use the rules (Ex: $A+B = \overline{\overline{A+B}} = \overline{\bar{A}\bar{B}}$)

Such as $\bar{\bar{A}} = A$ & Demorgan's Laws.

ⓒ Make sure we have one bull complement for the whole expression is present. If not put double bars ($\because A = \bar{\bar{A}}$)

④ Rules to be followed to implement using only NOR gates

Follow the above two steps [with '+' replaced by '·' & '·' replaced by '+']

① $0 \cdot A \oplus 0 \cdot B = 0$

② $1 + A \oplus 1 + B = 1$

③ NAND gate Latch

$\bar{S} = \bar{R} = 1$, $Q = NC$, $\bar{S} = \bar{R} = 0$, $Q = \bar{Q} = 1$ (Invalid)

$\bar{S} = 0 (\bar{R} = 1)$ Q = Set , $\bar{R} = 0 (\bar{S} = 1)$ Q = Reset

④ NOR gate Latch

$R = S = 0$, $Q = NC$, $R = 1 (S = 0)$, Q = Reset

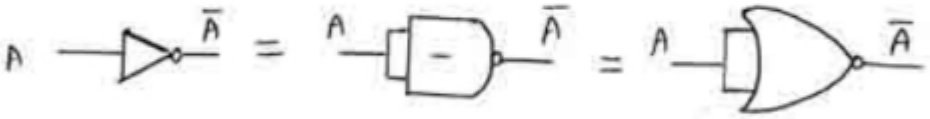
$R = 0 (S = 1)$, Q = Set , $R = S = 1$, $Q = \bar{Q} = 0$ (Invalid)

⑤ RS Flip flop

$R = S = 0$, $Q = NC$ $R = 1 (S = 0)$, Q = Reset

$R = 0 (S = 1)$, Q = Set $R = S = 1$, $Q = \bar{Q} = 1$ (Invalid)

⑥



⑦ Clocked RS Flip flop using NAND gate

$CLK = 0$, $S = X$, $R = X$, $Q = NC$

$CLK = 1$, $S = R = 0$, $Q = NC$

$CLK = 1$, $S = 0 (R = 1)$, Q = Reset

$CLK = 1$, $S = 1 (R = 0)$, Q = Set

$CLK = 1$, $S = R = 1$, $Q = \bar{Q} = 1$ (Invalid)

⑧ Clocked RS Flip flop using NOR gates

$CLK = 0$, $S = X$, $R = X$, $Q = NC$

$CLK = 1$, $S = R = 0$, $Q = NC$

$CLK = 1$, $S = 1 (R = 0)$, Q = Set

CLK = 1, S = 0 (R = 1), Q = Reset

CLK = 1, S = R = 1, Q = $\bar{Q}$ = 0

Microcontroller

$$\text{Step angle} = \frac{360}{\text{Number of steps per revolution}}$$

$$\text{RPM} = \frac{60 \times \text{Steps per second}}{\text{Steps per revolution.}}$$

① Height of antenna.

$$h = \frac{\lambda}{4} = \frac{c/f}{4} \quad [\because c = f\lambda]$$

② Message signal.

$$m(t) = V_m \sin \omega_m t$$

③ Carrier signal.

$$c(t) = V_c \sin \omega_c t$$

④ AM

Amplitude of AM wave.

$$A(t) = V_c + K_a V_m \sin \omega_m t = V_c + K_a m(t) \quad (\text{Let } K_a = 1)$$

AM wave:

$$v(t) = V_c \sin \omega_c t + \frac{V_m}{2} \cos(\omega_c - \omega_m)t - \frac{V_m}{2} \cos(\omega_c + \omega_m)t$$

Modulation index:

$$m = \frac{V_m}{V_c} \quad (0 \le m \le 1) \quad m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$$

Bandwidth: $BW = 2f_m (Hz)$ or $2\omega_m (rad/s)$ or USB - LSB

Total power: $P_t = P_{car}\left(1 + \frac{m^2}{2}\right)$, $P_{car} = \frac{V^2}{2R}$

Modulation index interms of P_t & P_{car} (I_t & I_{car}) or V_t & V_{car}):

$$m = \sqrt{2\left(\frac{I_t}{I_{car}}\right)^2 - 1} = \sqrt{2\left(\frac{V_t}{V_{car}}\right)^2 - 1} = \sqrt{2\left(\frac{P_t}{P_{car}} - 1\right)}$$

or $I_t = I_{car}\sqrt{1 + \frac{m^2}{2}}$ or $V_t = V_{car}\sqrt{1 + \frac{m^2}{2}}$

or $I_{car} = \frac{I_t}{\sqrt{1 + \frac{m^2}{2}}}$ or $V_{car} = \frac{V_t}{\sqrt{1 + \frac{m^2}{2}}}$

Minimum & maximum amplitude $V_{min} = V_c - V_m$, $V_{max} = V_c + V_m$

Modulation index when a carrier is AMPLitude modulated by several waves:

$$M_t = \sqrt{M_1^2 + M_2^2 + \cdots + M_n^2}$$

$$P_t = P_{car}\left(1 + \frac{M_t^2}{2}\right)$$

Amplitudes of USB & LSB

$$V_{USB} = \frac{MV_c}{2} = V_{LSB} =$$

Transmission efficiency

$$\eta = \frac{M^2}{2+M^2}$$

LSB & USB

$LSB = f_c - f_m$, $USB = f_c + f_m$

Time constant

$$\frac{2\pi}{\omega_c} << RC << \frac{2\pi}{\omega_m}$$

Detected envelope

$$V_d = V_c + MV_c \sin\omega_m t$$

$$\Rightarrow V_d = V_m \sin\omega_m t$$

5) FM

Instantaneous frequency of FM wave.

$$f_i = f_c(1 + K V_m \cos\omega_m t) = f_c \pm K f_c V_m$$

Angular frequency

$$\omega_i = \frac{d\theta_i}{dt}$$

Frequency sensitivity @ Deviation constant

$$K_f = K f_c$$

Frequency deviation

$$\Delta f = K_f V_m$$

$$\Delta f = K f_c V_m$$

FM wave.

$$v(t) = V_c \cos[(2\pi f_c t) + \beta \sin(2\pi f_m t)]$$

(or)

$$v(t) = V_c \sin[(2\pi f_c t) + \beta \cos 2\pi f_m t]$$

Modulation index (modulation factor) (phase deviation of FM)

$$\beta = \frac{\Delta f}{f_m} \text{ (or) } \frac{\Delta\omega}{\omega_m} \quad ; \quad \beta > 1$$

BW $\quad BW = 2(\Delta f + f_m) = 2\Delta f\left(1 + \frac{1}{\beta}\right) = 2f_m(\beta+1)$

$$= 2\beta f_m + 2f_m$$

Instantaneous phase

$$\theta_i = \omega_c t + \beta \sin(2\pi f_m t)$$

6 PM

Instantaneous phase of PM wave.

$$\theta_i = \omega_c t + m_p \cos \omega_m t$$

PM wave

$$v(t) = V_c \cos[2\pi f_c t + m_p \cos(2\pi f_m t)]$$

Modulation index

$$m_p = K_p V_m$$

BW

$$BW = 2f_m(1+m_p) = 2f_m(1+K_pV_m)$$

Transducer

1. Resistance (DC resistance) of any metal is,

$$R = \frac{\rho L}{A}$$

2. Resistance of resistance thermometer at T(°c) is,

$$R_T = R_0(1+\alpha T), \quad R_0 \rightarrow \text{Resistance at } 0^\circ c$$

$T \rightarrow$ Temperature in °C

$$\alpha = \frac{1}{\Delta T}\frac{\Delta R}{R_0}$$

3. Self-heating coefficient.

$$E = \frac{\Delta t}{R_T I^2}$$

4. Resistance of thermistor at T(K)

$$R = R_0 e^{\beta\left(\frac{1}{T} - \frac{1}{T_0}\right)} \simeq R_0 e^{\beta/T}$$

5. Output voltage of LVDT is,

$$V_o = V_{o1} - V_{o2}$$

3) Output voltage of Piezoelectric transducer

$$V_o = \frac{g t F}{A} = g t P \qquad \left(g = \frac{k}{t}\right)$$